



**2007 IEEE
Radio Frequency
Integrated Circuits
(RFIC) Symposium**

Honolulu, Hawaii — June 3-5, 2007



IEEE

PROGRAM

**Hawaii Convention Center
June 3-5, 2007**

Sponsored by
**IEEE Microwave Theory and Techniques Society
IEEE Electron Device Society
and
The IEEE Solid-State Circuits Society**



RFIC Plenary and Reception – Sunday Night (Sunday June 3, 2007)

After a busy day of outstanding RFIC Workshops (see page 88-99), the Plenary Session and RFIC Reception will be held on Sunday evening – June 3, 2007. These activities are the highlight of technical activities and social festivities. The evenings activities include the Plenary Session at 17:30 in the Hawaiian Convention Center Room 311. The Plenary Session will include two outstanding speakers (see page 8-9), and the Student Paper Award ceremony. The RFIC Reception will follow at 19:00 in the Convention Center’s Rooftop Gardens. All RFIC Symposium Attendees are invited to attend. An admission ticket good for attendee and spouse/guest to the Reception is included in the RFIC Registration Packet. Meeting attendees that do not register for the RFIC Symposium can purchase Reception Tickets at the symposium registration desk..

RFIC Weeks Activities (June 2-8, 2007)

- | | | |
|------|---------------|--|
| Sat: | 14:00 - 18:00 | Registration at Convention Center |
| Sun: | 07:00 - 18:00 | Registration at Convention Center |
| | 08:00 - 17:00 | RFIC and IMS Workshops |
| | 17:30 - 19:00 | RFIC Plenary |
| | 19:00 - 21:00 | RFIC Reception |
| Mon: | 07:00 - 18:00 | Registration at Convention Center |
| | 07:00 - 08:00 | Attendee Breakfast |
| | 08:00 - 17:10 | RFIC Technical Sessions (pages 10 to 41) |
| | 08:00 - 09:40 | RMO1A RMO1B RMO1C RMO1D |
| | 09:40 - 10:10 | Break |
| | 10:10 - 11:50 | RMO2A RMO2B RMO2C RMO2D |
| | 11:50 - 13:20 | Lunch Break/RFIC Panel Session |
| | 13:20 - 15:00 | RMO3A RMO3B RMO3C RMO3D |
| | 15:00 - 15:30 | Break |
| | 15:30 - 17:10 | RMO4A RMO4B RMO4C RMO4D |
| | 18:00 - 20:00 | Microwave Journal Reception |
| Tue: | 07:00 -18:00 | Registration at Convention Center |
| | 07:00 - 08:00 | Attendee Breakfast |
| | 08:00 - 17:10 | RFIC Technical Sessions (pages 42 to 65) |
| | 08:00 - 09:40 | RTU1A RTU1B RTU1C RTU1D RTU1E RTU1F |
| | 09:40 - 10:10 | Break |
| | 10:10 - 11:50 | IMS Plenary (RFIC Attendees are Invited) |
| | 11:50 - 13:20 | Lunch Break/RFIC Panel/IMS Panel |
| | 13:20 - 15:00 | RTU3A RTU3B RTU3C RTU3D |
| | 15:00 - 15:30 | Break |
| | 15:30 - 17:10 | RTU4A RTU4B RTU4C RTU4D |
| | 14:00 - 17:00 | RTUP (Interactive Forum) |

Information contained in this Program Book as well as additional information can be found on the RFIC website www.rfic2007.org

IMS Technical Sessions and the Industrial Exhibit are held on Tuesday-Thursday from 08:00 - 17:10. IMS-Program-Book details can be found at www.ims2007.org Details of the ARFTG Conference which is held on Friday can also be found on the IMS website. RFIC spouses/guests are invited to take advantage of the IMS Guest Program listed on the IMS website.

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The RFIC Symposium brings focus to the technical accomplishments in RF systems, circuit, device and packaging technologies for mobile phones, wireless communications systems, broadband access modems, radar systems and intelligent transport systems.

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Message from the General Chairman

Welcome to the 2007 RFIC Symposium!

The 2007 RFIC Symposium maintains its reputation as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development for wireless and wireline communication IC's. Running in conjunction with the International Microwave Symposium and Exhibition, the RFIC Symposium adds to the excitement of Microwave Week with three days focused exclusively on RFIC technology and innovation. The RFIC symposium will be held at the Hawaii Convention Center, from 3-5 June, 2007.



Luciano Boglione

The symposium begins on Sunday, 3 June with workshops targeted at RF technology, design, and system issues. Sunday evening activities continue at 17:30 with the Plenary Session where 2 speakers will share their views on the direction and challenges that the RF IC industry will be facing. The first speaker, Charles Persico, Senior Vice President of Engineering at Qualcomm Inc., will discuss "Wireless Convergence – Your Phone is Not Just a Phone Anymore." The second speaker, Dwight C. Streit, Ph.D., Vice President, Electronics Technology, Northrop Grumman Space Technology, will discuss "Technology Directions for Future RF Applications." Following the Plenary Session, the RFIC reception will be hosted on the Convention Center Rooftop Garden. This social event is a key component of the conference with the opportunity to connect with old friends and new acquaintances and catch up on the wireless industry. The technical program includes oral sessions, an Interactive Forum, and two lunch time panel sessions. The technical program formally starts on Monday, 4 June with four parallel oral sessions in the morning and in the afternoon. More technical sessions are planned on Tuesday, 5 June to accommodate the all-time record number of papers the RFIC symposium has received this year. The Interactive Forum will be held on Tuesday afternoon. The IF session is the perfect place to have an opportunity to have more detailed technical discussions with the authors. In the tradition of the RFIC conference, the Tuesday morning activity will be paused during the IMS Plenary Session, from 10:10 -11:50. Panel Sessions are also planned at lunch time on Monday and Tuesday. The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall. The RFIC organization is thankful to the Microwave Week team, without whom we could not make this conference happen. Most of all, we are particularly thankful to all the technical contributors to the RFIC. We look forward to your participation. Please continue to make this conference so vibrant within the wireless industry!

Enjoy the conference!

Luciano Boglione
General Chairman
2007 RFIC Symposium

Message from the Technical Program Committee Chairs



Jenshan Lin



Tina Quach

On behalf of the Technical Program Committee, welcome to the 2007 IEEE RFIC Symposium. The RFIC Symposium is a leading-edge IEEE technical conference dedicated to the advancement of integrated circuits and sub-systems for RF, wireless, broadband communications, and many other emerging applications. This year the number of paper submissions reached an all-time record number of 349 papers, following an increasing trend since the inauguration of RFIC Symposium in 1997. The RFIC Technical Program Committee has worked diligently to select the best papers to assemble a high quality technical program this year. These papers will be presented in 31 technical sessions – the largest number of sessions RFIC Symposium ever had. RFIC Symposium also features a student paper contest. Three best student papers will be selected by the Technical Program Committee and the awards will be presented in the Plenary Session. This year the RFIC Symposium begins on Sunday, 3 June with workshops at the advanced and tutorial level addressing RF technology, design and integration, at both system and circuit levels. The Plenary Session will be held on Sunday evening, following the workshops. Two leading experts from RFIC industry will share their views during the plenary session. The RFIC Reception will follow immediately after the plenary session, providing a relaxing time for all to mingle with old friends and catch up on the latest news. In addition to the technical sessions on Monday and Tuesday, the RFIC Symposium also features 2 Panel Sessions and 15 Workshops. A panel session entitled “RFID: New Revolution or Re-Marketing of Existing Technologies in a New Package?” will take place during lunch on Monday and have panelists from both industry and academia offer their views on the challenges ahead. Another panel session on Tuesday, “CMOS Millimeter-Wave MMIC, Real or Bubble?” is posed to allow for many interactive discussions with the audience! The workshops on Sunday cover a wide range of topics from system to device technologies.

The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to be the venue of choice for both industry and academia to meet, discuss results and exchange ideas. The 2007 Technical Program Committee keeps working diligently toward the goal of strengthening the technical quality and scope of the program, while maintaining and improving the legacy left by the previous Symposia. This would not be possible without keeping the interest of professionals like you and gaining the trust of all the authors who submitted their work to the RFIC Symposium.

We hope you enjoy the 2007 RFIC Symposium!

Jenshan Lin and Tina Quach
Technical Program Chairs
2007 IEEE RFIC Symposium

Steering Committee

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Luciano Boglione, Custom One Design

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RFIC Schedule 2007

The RFIC Symposium will be held in the Hawaiian Convention Center, Honolulu, HI. The headquarters hotel is the Hilton Hawaiian Village. The RFIC Plenary and Reception will be held on Sunday June 3 at the Convention Center. The Plenary will be in room 311 and the Reception will follow in the HCC Roof Top Garden.

The RFIC Symposium is held in conjunction with the International Microwave Symposium (IMS). Attendees of the RFIC Symposium are invited to attend the IMS Plenary Session on Tuesday June 5 and MTT Social Events.

Saturday June 2, 2007

14:00 - 18:00 Registration –
Hawaiian Convention Center (HCC)

Sunday June 3, 2007

07:00 - 18:00 Registration – HCC
08:00 - 17:00 Workshops – HCC
08:00 - 17:00 Tutorials – HCC
17:30 - 19:00 Plenary – HCC Room 311
19:00 - 21:00 RFIC Reception
HCC – Roof Top Garden

Monday June 4, 2007

07:00 - 17:00 Registration – HCC
07:00 - 08:00 Speakers Breakfast
HCC – Room 323ABC
07:00 - 08:00 Registered Attendee Breakfast
HCC – Main Lobby
07:00 - 17:00 Speakers Preparation
HCC – Room 325A
08:00 - 09:40 RFIC Oral Technical Sessions
HCC – See Listings
09:40 - 10:10 Break – HCC
10:10 - 11:50 RFIC Oral Technical Sessions
HCC – See Listings
11:50 - 13:20 RFIC Panel
HCC – Room 313C
13:20 - 15:00 RFIC Oral Technical Sessions
HCC – See Listings
15:00 – 15:30 Break – HCC
15:30 – 17:10 RFIC Oral Technical Sessions
HCC – See Listings
18:00 – 20:00 Microwave Journal Reception
HCC – Roof Top Garden

RFIC Schedule (Continued)

Tuesday June 5, 2007

07:00 - 17:00	Registration – HCC
07:00 - 08:00	Speakers Breakfast HCC – Room 323ABC
07:00 - 08:00	Registered Attendee Breakfast HCC – Main Lobby
07:00 - 17:00	Speakers Preparation HCC – Room 325A
08:00 - 09:40	RFIC Oral Sessions HCC – See Listings
09:40 -10:10	Break HCC – Exhibits Area
10:10 - 11:50	MTT Plenary Session HCC – Ballroom BC
11:50 - 13:20	RFIC Panel HCC – Room 313C IMS Panel HCC – Room 316C
13:20 - 15:00	RFIC Oral Sessions
14:00-17:00	RFIC Interactive Forum (RTUP) HCC-Ballroom A
15:00-15:30	BREAK
15:30-17:10	RFIC Oral Sessions

Sunday, June 3, 2007 – 5:30 PM

HCC – Room 311

Session RSU5A: RFIC Plenary

Session Chair: Luciano Boglione, Custom One Design

Session Co-Chairs: Jenshan Lin, University of Florida
and Tina Quach, Freescale Semiconductor Inc.

17:30	Welcome message from General and TPC Chairs, Announcement of Student Paper Awards
17:45	RSU5A-1: Wireless Convergence – Your Phone is Not Just a Phone Anymore Charles Persico, Qualcomm, Inc., San Diego, CA
18:15	RSU5A-2: Technology Directions for Future RF Applications Dwight Streit, Northrop Grumman Space Technology, Redondo Beach, CA



**RSU5A-1:
Wireless Convergence –
Your Phone is not Just a
Phone Anymore**

Charles Persico
Vice President of Engineering,
Qualcomm, Inc.

A look at wireless convergence in the mobile phone market goes beyond voice to photography, video, gaming, music, multimedia broadcast, Internet access, position location, VOIP, WiFi, Bluetooth to name several. It has only been a few years since voice only cellular mobile phones have become ubiquitous and considered indispensable in our daily lives.

What is the future direction for integration of multiple radios' and concurrent operation between various protocols.

Charles Persico is Senior Vice President of Engineering at Qualcomm Inc. Charlie is in charge of all Qualcomm's RF, analog and mixed signal IC design, product and test engineering and responsible for more than a billion dollar revenue business, which makes Qualcomm the largest RF, analog and mixed signal IC supplier in the world. Charlie was born in 1960 in Schenectady, NY. He received his BS from Union College in electrical engineering in 1985 and MS from Syracuse University in electrical engineering in 1987. In 1985 he joined GE Avionics systems working on advanced radar systems. He also worked at Honeywell Space Systems on various satellite electronic systems. In 1991 he joined Philips Semiconductor and was involved in RFIC design for various cellular standards. He has been with Qualcomm since 1995 and led all Qualcomm's RF, analog and mixed signal IC product development and production.



RSU5A-2: Technology Directions for Future RF Applications

Dwight C. Streit, Ph.D.
Vice President, Electronics Technology,
Northrop Grumman Space
Technology

Recent advances in the performance and maturity of a number of key technologies are enabling a new generation of electronic systems for future RF applications. Advanced semiconductors, photonics and nanotechnology are converging with new design, processing and packaging schemes to revolutionize RF system performance. Millimeter-wave circuits now operate above 300 GHz and digital circuits above 100 GHz. Monolithic integration of MEMS and HEMT devices enables intelligent circuits that can adapt to their environment. Low-power InSb devices enable microwatt receivers, while high-power GaN devices enable kilowatt transmitters. Microwave transceivers built using wafer-level micropackages reduce size and weight by a factor of 100, enabling new phased-array and other applications. We present here an overview of the key technologies behind these achievements, and discuss their impact to future electronic systems.

Dwight Streit is vice president, Electronics Technology, for Northrop Grumman Space Technology. He is responsible for the research and technology development required for advanced semiconductors, microelectronics, communications and satellite payload electronics. Dr. Streit joined Northrop Grumman via the acquisition of TRW in 2002, he joined TRW Space & Electronics in 1987. He is an IEEE Fellow and a member of the National Academy of Engineering. He received his Ph.D. in electrical engineering from UCLA in 1986, and was the UCLA Engineering Alumnus of the Year in 2003.

Monday June 4, 2007

08:00

Room: HCC - 313A

Session RM01A: Cellular Transceivers

Chair: Fazal Ali, Qualcomm

Co-Chair: Jyoti P. Mondal, Freescale

RM01A-1 08:00 Room: HCC-313A

INVITED: Single Chip Cellular Radios for GSM,GPRS, EDGE

D. Seippel, M. Hammes, J. Kissing, P. de Nicola*, C. Vannier**, Infineon Technologies, Duisburg, Germany, *Infineon Technologies, Sophia-Antipolis, France, **Infineon Technologies, Xi'an, China

Nowadays CMOS Baseband-radios for GSM/GPRS application are running in high-volume production. The next step for higher integration is the integration of the Power-Management Unit (PMU) and extending the functionality towards EDGE capabilities. This extended integration promises lower production cost, easier board design and the highest flexibility in system optimization. In this paper we will present both features as highest integrated solutions for cellular phones.

RM01A-2 08:20 Room: HCC-313A

Integrated Blocker Filtering RF Front Ends

A. Safarian*, A. Shameli*, A. Rofougaran**, M. Rofougaran**, F. De Flaviis*. * University of California, Irvine, CA. ** Broadcom Corporation, Irvine, CA.

The paper presents integrated blocker filtering RF front-ends (BF-RF) for wireless cellular systems. The proposed BF-RF deploys the concept of blocker injection using feedforward or feedback paths to create arbitrary narrowband notches to reject the blockers, but not affecting the gain of the desired signal. Fabricated in a 0.18 um CMOS technology the prototype achieves a 50dB of signal to blocker ratio.

RM01A-3 08:40 Room: HCC-313A
A 90nm CMOS Direct Conversion Transmitter for WCDMA

X. Yang, *A. B. Davierwalla, **D. W. Mann, K. G. Gard, North Carolina State University, *Qualcomm, Inc., **IBM, Inc.

A linear high output power CMOS direct conversion transmitter for wide band code division multiple access (WCDMA) is presented. Circuit level third order distortion cancellation is applied to driver amplifier to achieve single end output power +9.6 dBm with -43.2dBc ACLR@5Mhz and 10% power efficiency at band II. The transmitter is fabricated in 90nm CMOS technology and die area is 1.1mm X 1.4mm. The VDD supply for upconverter is 1.4V, and the VDD for driver amplifier is 3V.

RM01A-4 09:00 Room: HCC-313A
A Superheterodyne Receiver Front-End With On-Chip Automatically Q-Tuned Notch Filters

B. Chi, Z. Wang, S. S. Wong*, Tsinghua University in China, *Stanford University in U.S.A.

A superheterodyne receiver front-end with on-chip automatically Q-tuned notch filters is proposed. The front-end includes a differential LNA and a Gilbert down-converter, each block is coupled with an on-chip image-rejection notch filter to get high image-rejection ratio. The notch filter is formed by one LC network and one negative-resistance cross-coupled pair to compensate the loss of the LC network. The current through the cross-coupled pair is automatically adjusted by a master Q tuning circuit.

RM01A-5 09:20 Room: HCC-313A
A Dual-band High Efficiency CMOS Transmitter for Wireless CDMA Applications

J. Deng, M. Chew, S. Vora, M. Cassia, T. Marra, K. Sahota, Qualcomm Inc

A dual-band TxIC, including BB filter and VGA, upconverter, RF VGA, and DA, is implemented in 0.18um CMOS for CDMA applications. The TxIC increases the handset talk time dramatically with the PA-bypass feature. The chip provides more than a total power control range of 80dB and a fine gain step of 0.25dB/LSB. The chip achieves 52.3dBc ACPR at +7dBm output power with 52.2mA and 50.4dBc ACPR at +7dBm output power with 51.9mA for low band and high band applications respectively.

Monday June 4, 2007

08:00

Room: HCC - 313B

Session RM01B: Pulsed UWB Transceivers

Chair: Ranjit Gharpurey, University of Texas, Austin

Co-Chair: Madhukar Reddy, Maxlinear

RM01B-1 08:00 Room: HCC-313B

A 10GS/s 5-bit Ultra-Low Power DAC for Spectral Encoded Ultra-Wideband Transmitters

J. I. Jamp, J. Deng, L. E. Larson, University of California at San Diego

A 5-bit 10Gs/s DAC for Spectral Encoded UWB transmitters is presented. A test counter is integrated on-chip to facilitate performance measurement. The chip has dimensions of 1.0x1.5mm, and is implemented in a 0.18 μ m SiGe BiCMOS process. The DAC operates conversion rates of over 10Gs/s with a power dissipation of 12mW. Linearity results of the DAC at 5GS/s are presented, with the DNL < ± 0.5 LSB and INL < ± 0.8 LSB.

RM01B-2 08:20 Room: HCC-313B

A 10GS/s Distributed Waveform Generator for Sub-Nanosecond Pulse Generation and Modulation in 0.18 μ m Standard Digital CMOS

Y. Zhu, J.D. Zuegel, J.R. Marciante, H. Wu, University of Rochester

A distributed waveform generator is presented for sub-nanosecond pulse generation in UWB impulse radios. It time-interleaves multiple digital pulse generators, and uses an on-chip transmission line for wideband pulse combining. Compared to other UWB pulse generation and shaping solutions, it is low power and fully reconfigurable. A 10-tap, 10GS/s prototype was implemented in 0.18 μ m standard digital CMOS. It consumes 50mW at 1GHz pulse repetition rate. On-off keying modulation is demonstrated.

RM01B-3 08:40 Room: HCC-313B

A Fully Integrated CMOS Transmitter for Ultra-wideband Applications

T. Yuan, Y. J. Zheng*, C. W. Ang**, L. W. Li**, National University of Singapore, *Institute of Microelectronics, Singapore., **National University of Singapore.

In this paper, a fully integrated CMOS UWB transmitter is presented. The transmitter consists of a band-notched UWB antenna and a transmitter IC which integrates a pulse generator, a gating signal generator and driver amplifiers. Fabricated using a 0.18- μ m CMOS process, the generated pulse is then passed through the driver amplifier (DA) which not only drives the antenna but also shapes the generated digital pulse in the FCC spectral mask.

RM01B-4 09:00 Room: HCC-313B
65nm CMOS Burst Generator for Ultra-Wideband Low Data Rate Systems

D. Marchaland, F. Badets, M. Villegas*, D. Belot, STMicroelectronics, *ESIEE Paris

This paper presents a burst generator architecture dedicated to UWB communication systems based on Impulse Radio principle. Bursts are generated by using an oscillator output signal controlled both in magnitude and phase with a high-speed digital circuit in order to limit output signal bandwidth in accordance with IEEE 802.15.4a standard requirements. The design has been integrated on a single-chip in the 65nm CMOS STMicroelectronics technology under a 1.2V voltage and measurement are presented.

RM01B-5 09:20 Room: HCC-313B
A 0.18- μ m CMOS UWB LNA with 5 GHz Interference Rejection

Y. Gao* **, Y.J. Zheng*, B.L. Ooi**, * Institute of Microelectronics, ** National University of Singapore

A ultra-wideband low noise amplifier (LNA) with integrated notch filter for interference rejection is designed using 0.18- μ m CMOS technology. The three-stage LNA employs a current reuse structure to reduce the power consumption and a serial LC circuit with Q-enhancement circuit to produce band rejection in the 5-6GHz frequency band. The load tank optimization for the current reuse stage is discussed for gain flatness tuning.

Monday June 4, 2007

08:00

Room: HCC - 316B

**Session RM01C: Broadband and Reconfigurable
CMOS LNAs**

Chair: Kirk Ashby, Microtune

Co-Chair: Dan Nobbe, Peregrine Semiconductor

RM01C-1 08:00 Room: HCC-316B

**A 1.2 V, Inductorless, Broadband LNA in 90 nm
CMOS LP**

M. Vidojkovic, M. Sanduleanu*, J. Van der Tang**, P. Baltus***, A. van Roermund, Eindhoven University of Technology, The Netherlands, *Philips Research Europe, **Holst Centre/IMEC-NL, ***Innovation Center RF, NXP Semiconductors, NL

This paper presents a novel broadband, inductorless, resistive–feedback CMOS LNA. The LNA is designed for the frequency band 0.4 – 1GHz. The measured power gain of the LNA is 16dB at 1GHz and the 3-dB bandwidth is 2 GHz. A noise figure of 3.5dB and an II_3 of -17 dBm are measured at 900 MHz. The S_{11} is better than -10 dB in the frequency band from 300MHz up to 1GHz. The current consumption is 14mA from a 1.2V supply. The circuit is designed in a baseline CMOS 90nm Low Power (LP) process.

RM01C-2 08:20 Room: HCC-316B

**A 12 mW, 7.5 GHz Bandwidth, Inductor-less CMOS
LNA for Low-Power, Low-Cost, Multi-Standard Receivers**

B. G. Perumana *&**, J-H. C. Zhan *&***, S. S. Taylor*, J. Laskar**, *Intel Corporation, ** Georgia Electronic Design Center, Georgia Institute of Technology, ***RF Division, MediaTek

A resistive feedback LNA is presented based on a current-reuse transconductance-boosting technique that reduces the power consumption to 12 mW. It has a gain of 21 dB and a noise figure of 2.6 dB at 5 GHz. The LNA achieves an output- IP_3 of 12.3 dBm at 5GHz by reducing loop-gain roll-off and by improving linearity of individual stages. The active die area of 0.012 mm-square is the lowest reported for an LNA.

RM01C-3 08:40 Room: HCC-316B

A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation

W. Chen*, G. Liu*, B. Zdravko**, A. Niknejad*, *Berkeley Wireless Research Center, University of California, Berkeley, CA, **Infineon Technologies, Munich, Germany

This paper presents a broadband very low 3rd-order intermodulation inductor-less low-noise amplifier (LNA) implemented in 0.13 μm CMOS technology. Broadband input matching, noise and distortion cancellation techniques are applied in this LNA to achieve +6dBm IIP₃ in both the 900MHz and 2GHz bands while maintaining minimum internal gain 14.5dB and noise figure below 2.6dB from 800MHz-2.1GHz. The LNA draws 11.6mA from a supply of 1.5V.

RM01C-4 09:00 Room: HCC-316B

A 2.4 to 5.4 GHz Low Power CMOS Reconfigurable LNA for Multistandard Wireless Receiver

C. T. Fu, C. L. Ko, C. N. Kuo, National Chiao-Tung University at Hsinchu, Taiwan

A CMOS reconfigurable LNA is reported. By combination of switched inductors and varactors it performs continuous frequency tuning from 2.4 to 5.4 GHz with 500MHz 3dB-bandwidth. Switching transistor is used to provide variable gain over 12dB-range. The LNA supports standards including Bluetooth, WiMAX, UWB mode-1, 802.11b/g and part of 802.11a. Fabricated in 0.13 μm CMOS process it achieves up to 25dB power gain, 2.2dB noise figure, -1dBm IIP₃ while consuming less than 5mW from 1V power supply.

RM01C-5 09:20 Room: HCC-316B

A Multi-band 900MHz/1.8GHz/5.2GHz LNA for Reconfigurable Radio

V. Kien Dao, Q. D. Bui, C. S. Park, School of Engineering, Information and Communications University (ICU)

A multi-band 900MHz/1.8GHz/5.2GHz low noise amplifier (LNA) which can operate at mobile band of 900MHz and 1.8G and WLAN band of 5.2GHz frequency is proposed. Input matching, noise matching and narrow gain are achieved at three frequency bands by adopting a switched output load and a resistive shunt-feedback circuit. The LNA has gain of 14 dB, 13 dB and 16 dB; noise figure of 2.3 dB, 2.9 dB and 2.7 dB at 900 MHz, 1.8 GHz and 5.2 GHz frequency band respectively while dissipating power of 7.5 mW.

Monday June 4, 2007

08:00

Room: HCC - 316A

Session RM01D: PAs for Wireless Connectivity

Chair: David Ngo, RFMD

Co-Chair: Noriharu Suematsu, Mitsubishi Electric

RM01D-1

08:00

Room: HCC-316A

A WCDMA HBT Power Amplifier Module with Integrated Si DC Power Management IC for Current Reduction Under Backoff Operation

G. Hau, J. Turpel, J. Garrett, H. Golladay, Fairchild Semiconductor Corp.

A 3x5mm WCDMA PA module integrated with GaAs PA and Si BiCMOS DC power management IC is presented. The IC contains an adaptively controlled DC-DC buck converter for optimizing the PA collector voltage under backoff operation, and an LDO regulator which supplies an internally regulated PA bias voltage. The PAM achieves excellent current reduction over a wide range of Pout. At 16dBm and 24dBm, the current consumptions are reduced from 162mA and 370mA, to 75mA and 257mA over conventional design.

RM01D-2

08:20

Room: HCC-316A

A Flip-Chip Silicon IPMOS Power Amplifier and a DC/DC Converter for GSM 850/900/1800/1900 MHz Systems

A. Tombak, R. J. Baeten, J. D. Jorgenson, D. C. Dening, RF Micro Devices Inc.

An LDMOS-based MOS device, called Integrated Power MOS (IPMOS), was developed to provide integration of high-performance reliable RF power devices with the rest of the front-end using flip-chip packaging. A 3-stage power amplifier (PA) die containing 1-830 and 1-8-40 mm wide IPMOS devices was designed for GSM 1800/1900 and GSM 850/900 MHz systems, respectively. The PA for GSM 850/900 achieved power added efficiencies (PAE) in the range of 54 to 62% across the band with output power (Pout) ranging from 34.5 to 35.4 dBm when driven with input power (Pin) greater than 3 dBm. The PA for GSM 1800/1900 achieved PAEs in the range of 39 to 42% with Pout ranging from 32.5 to 33.7 dBm when driven with Pin greater than 4 dBm. A DC/DC buck converter was also designed using the same process, and the bias to the PA for GSM 850/900 was applied through this converter. PAEs when Pin and DC/DC converter output voltage are varied were compared. We are currently working towards the integration of the PA with the converter, and hope to publish data including PAE, receive band noise and spurious response during the final submission/conference.

RM01D-4 08:40 Room: HCC-316A

**A Compact Dual-Band Power Amplifier Driver for
2.4GHz and 5.2GHz WLAN Transmitters**

H. Magnusson, H. Olsson, Royal Institute of Technology

This paper presents a dualband power amplifier driver with matched output operating in the 2.4GHz/5.2GHz bands. The use of tunable differential inductors both in the RF choke and the matching circuit saves significant die-area compared to traditional configurations of integrated PA drivers. The fabricated circuit size is as small as 0.48mm^2 for the used $0.18\mu\text{m}$ CMOS process, saving about 0.5mm^2 silicon area. Measurement results shows a maximum gain and output power of 10.4dB and 13dBm, respectively.

RM01D-5 09:00 Room: HCC-316A

**A 3.5 GHz 25 W Silicon LDMOS RFIC Power Amplifier
for WiMAX Applications**

C. Cassan, P. Gola, Freescale Semiconductors, Inc., Toulouse, FRANCE

This paper presents a 25 W Silicon LDMOS 2 stage RF integrated circuit (IC) designed for WiMAX at 3.5GHz. This paper details RF performances in the 3.4 to 3.6 GHz band. Under a 1 tone CW stimulus, this power amplifier delivers 29 W with a power added efficiency of 36.7% and 26 dB linear gain. Under a 1 carrier WiMAX signal and at 36 dBm average output power, the device has a RCE better than -33.5 dBc and a 14% drain efficiency typical.

Monday June 4, 2007

10:10

Room: HCC - 313A

Session RM02A: Power Efficient Transceivers

Chair: Derek Shaeffer, Beceem Communications

Co-Chair: Steve Lloyd, Beceem Communications

RM02A-1 10:10 Room: HCC-313A

INVITED: CMOS Radio with an Integrated 26dBm Power Amplifier for a Complete System-on-Chip Cordless Phone

C.Grewing, S.vanWaasen*, B.Bokinge, W.Einerman, A.Emericks, R.Engberg, C.Hedenäs, H.Hellberg, M.Hjelm, S.Irmscher, T.Johansson, A-M.Lann, M.Lewis, B.Li, O.Petterson, W.Simbürger*, D.Theil, R.Thüringer*, Infineon Tech. Nordic Sweden, *Infineon Tech. Germany

A fully integrated transceiver in a 0.13 μ m CMOS technology including on-chip Power Amplifier (PA) for digital cordless telephone standards is presented. The PA exhibits an output power of $POUT = 26\text{dBm}$. The receiver is measured to achieve a sensitivity level of $PO.1\% = -96\text{dBm}$. The PA shows a power added efficiency (PAE) of more than 30% at a $VPA = 2.5\text{V}$ direct-connect-to-battery supply. The transceiver is developed as a part of a complete System-on-Chip (SoC) cordless phone.

RM02A-2 10:30 Room: HCC-313A

A Sub-10mW 2 Mbps BFSK Transceiver at 1.35 to 1.75GHz

T. M. Hancock, M. Straayer, A. Messier, MIT Lincoln Laboratory

This work presents the design and measurement of a 2Mbps BFSK transceiver at 1.35 to 1.75GHz for wireless sensor node applications. The receiver has a sensitivity of -74dBm at 2Mbps and consumes 8.0mW while the transmitter generates orthogonal BFSK modulation through the use of digital pre-emphasis of the frequency control word and consumes 9.7mW. The transmitter delivers $>3\text{dBm}$ of output power for a total transmitter power efficiency of of 23% and a transmitter FOM of 4.85nJ/bit at 2Mbps.

RM02A-3 10:50 Room: HCC-313A
A 6.3 GHz BFSK Transmitter with On-Chip Antenna for Self-Powered Medical Sensor Applications

V. Karam, P. H. R. Popplewell, A. Shamim, J. Rogers, C. Plett, Department of Electronics, Carleton University, Canada

A completely integrated, low-power 6.3 GHz oscillator transmitter which includes an on-chip antenna is presented. The 1.2 V 0.13 μm CMOS transmitter uses BFSK modulation at a rate of 300 kbps. For communicating a 1 kbit packet once per second, the average power consumption is 14 μW . During a packet transmission, the power consumption is 4.25 mW, enabling a self-powered design using integrated ultracapacitors for an SoC solution. With a radiated power of 0 dBm, the transmitter's range is 2 m.

RM02A-4 11:10 Room: HCC-313A
A 0.13- μm CMOS Ultra-Low Power Front-End Receiver for Wireless Sensor Networks

W. Chen, T. Copani, H. J. Barnaby, S. Kiaei, Arizona State University

This paper presents an ultra-low power monolithic CMOS RF receiver, consisting of current re-use common gate LNA with inductive feedback gm-boosting, and followed by balanced I/Q mixers. The receiver is fabricated in the IBM 0.13- μm CMOS digital process operating at 2.45 GHz. The measurement results show that the RF receiver achieves a gain of 20 dB and a noise figure of 7.5 dB at 2 MHz. Input 1-dB compression point is -19 dBm and IIP3 is -10 dBm, with 0.4 mA total current consumption from a 1.5-V supply

RM02A-5 11:30 Room: HCC-313A
A 0.5 V Receiver in 90 nm CMOS for 2.4GHz Applications

N. Stanic, A. Balankutty, P. Kinget, Y. Tsvividis, Columbia University

We report an ultra-low voltage RF receiver for applications in the 2.4GHz band, designed in 90nm CMOS technology. The sliding-IF receiver prototype includes an LNA, an image-reject LC filter/balun, RF and IF mixers with LO buffers, and an I/Q baseband section with a VGA and an LP channel-select filter in each path, all integrated on-chip. It has a programmable overall gain of 30dB, NF of 18dB, IIP3 of -22dBm, and 26dB of on-chip image rejection. The 3.4mm² chip consumes 8.5mW from a 0.5V supply.

Monday June 4, 2007

10:10

Room: HCC - 313B

Session RM02B: Voltage Controlled Oscillators

Chair: Tian-Wei Huang, National Taiwan University

Co-Chair: Lars Jansson, Tumbledown Technical Inc.

RM02B-1 10:10 Room: HCC-313B

A 10GHz Distributed Voltage Controlled Oscillator for WLAN Application in a VLSI 65nm CMOS Process

N. Seller, A. Cathelin, H. Lapuyade*, J.-B. Bégueret*,

E. Chataigner and D. Belot, STMicroelectronics - FTM - Crolles,

*IXL Laboratory - University of Bordeaux, France

This work demonstrates the feasibility of a Distributed Voltage Controlled Oscillator (DVCO) designed for WLAN applications in a 65 nm CMOS process with standard VLSI backend. This DVCO achieves a tuning range of 1.1GHz (from 10.6GHz to 11.7GHz) and a measured phase noise of -116dBc/Hz at 1MHz offset from the carrier. To achieve such performances, the DVCO consumes a DC current of 36mA from a 2V power supply.

RM02B-2 10:30 Room: HCC-313B

A Q-band Low Phase Noise Voltage Controlled Oscillator Using Balanced pi-Feedback in 2-micron GaAs HBT Process

C.-H. Lin, K.-H. Liang, H.-Y. Chang, Y.-J. Chan, C.-C. Chiong*,

E. Bryerton**, National Central University, *Academia Sinica, Institute of Astronomy and Astrophysics, **National Radio Astronomy Observatory

A Q-band low phase noise VCO using balanced-feedback in a 2-um GaAs HBT process is reported in this paper. The VCO features a phase noise of -105.5 dBc/Hz at 1-MHz offset, and a tuning frequency of from 41.2 to 42.1 GHz. The differential outputs are also provided from the VCO due to the use of balanced-feedback. The chip size of the VCO is 1x1 mm². To the best authors' knowledge, this work demonstrates the lowest FOM among all the reported VCOs except the InP-based HBT VCOs around 40 GHz.

RM02B-3 10:50 Room: HCC-313B
An X-Band Superharmonic Injection-Coupled Quadrature VCO (IC-QVCO) with a Tunable Tail Filter for I/Q Phase Calibration

I. R. Chamas, S. Raman, Wireless Microsystems Laboratory, Bradley Dept. of ECE, Virginia Tech, Blacksburg, VA

An X-band phase-tunable injection-coupled quadrature oscillator topology (PTIC-QVCO) for low power low phase noise quadrature signal synthesis is introduced. As a proof of concept, a 9 GHz prototype is implemented in a 0.18 μ m RF CMOS process, and achieves a measured phase noise figure of merit (FoM) ranging from 177.3 to 182.6 dBc/Hz along the 9.0 to 9.6 GHz frequency tuning range while draining only 5mA from a 1.8V power supply. Precise quadrature phase is achieved via the tuning technique

RM02B-4 11:10 Room: HCC-313B
A 2.4-GHz LC-Tank VCO with Minimum Supply Pushing Regulation Technique

X. Wang, B. Bakkaloglu*, Cadence Design Systems, Inc., *Arizona State University

Design of LDO regulated LC-tank VCO is presented. Low-frequency supply sensitivity of VCO phase noise is derived. LDO output noise and PSR profile is optimized by shaping the LDO AC response and tuning the ESR of the bypass capacitor while achieving maximum efficiency. The implemented regulated VCOs achieve less than 95dBc/Hz phase noise at 100kHz offset with 2.2mA current consumption. The VCO phase noise sensitivity to supply is improved by 30dB for offset frequency up to 10MHz with no peaking.

RM02B-5 11:30 Room: HCC-313B
2 GHz CMOS Voltage Controlled Oscillator with Optimal Design of Phase Noise and Power Dissipation

D. J. Young, S. J. Mallin, M. Cross, Case Western Reserve University

An RF VCO design optimization strategy to achieve low phase noise and low bias current is presented for a cross-coupled LC CMOS oscillator. An optimal trade-off between phase noise and DC power dissipation can be achieved when the oscillation amplitude is designed to set the cross-coupled transistors at the boundary between saturation and triode. A 2GHz VCO in a 0.18 μ m CMOS process achieves a phase noise of -103dBc/Hz at 100kHz offset frequency while dissipating 2.67mA from a 1.8V supply.

Monday June 4, 2007

10:10

Room: HCC - 316B

Session RM02C: Millimeter Wave Front-Ends

Chair: Georg Boeck, Berlin University of Technology

Co-Chair: Reynold Kagiwada, Northrop Grumman

RM02C-1 10:10 Room: HCC-316B

**40GHz Low Noise Receiver Circuits using
BCB Above-Silicon Technology Optimized for
millimeter-wave Applications**

S. Pruvost, R. Cuchet*, D. Pellissier, I. Telliez, M. Devulder, X. Gagnard,
P. Ancey, M. Aid*, F. Danneville**, G. Dambrine**, N. Rolland**,
S. Lepilliet**, STMicroelectronics, *CEA-Leti, MINATEC, **IEMN,
UMR

The building blocks of a 40GHz receiver were realized in a BCB post-processing and 0.13 μ m SiGe:C BiCMOS technology. The 2 stage LNA exhibits 2.2dB noise figure and 17dB of gain at 40GHz. This impressive performance in terms of noise demonstrate the advantage of the post-processed over standard BEOL passive elements, and also the intrinsic performance of the HBT (noise figure/gain) at millimeter-wave frequencies.

RM02C-2 10:30 Room: HCC-316B

**A 60-GHz Double Balanced Gilbert Cell Down
Conversion Mixer on 130nm CMOS**

F. Zhang, E. Skafidas, W. Shieh, National ICT Australia, Department of Electrical and Electronic Engineering, University of Melbourne, Parkville, Australia

Homodyne receiver structures enable low cost integrated transceivers. A critical requirement of these systems is a high isolation mixer. In this paper, a high LO to RF isolation, double-balanced (Gilbert Cell) 60-GHz down-conversion mixer is presented. This mixer achieves a voltage conversion gain better than 2 dB, input-referred IP₃ point of -8 dBm and LO to RF isolation greater than -36 dB when driven with a LO input of 0 dBm.

RM02C-3 10:50 Room: HCC-316B
A 77-GHz Receiver Front-End for Passive Imaging

J. Powell, H. Kim*, C. G. Sodini, Massachusetts Institute of Technology,
*MIT Lincoln Laboratory

A 77-GHz Front End Receiver for Passive Imaging has been characterized. This system comprises an LNA, Mixer and VCO. The LNA achieves 4.9-6.0 dB NF, 18-26 dB gain, and S11, S22 of -13.0 and -12.8 dB, respectively. The Mixer achieves 12-14 dB NF, 20-26 dB gain and -26dBm P1dB (input-referred). The VCO achieves output power from -2 to 0 dBm with phase noise of ~ -93 dBc/Hz at 72 GHz, and 3 GHz of tuning range. The receiver achieves 40-46 dB max gain, output P1dB of 2 dBm, and dissipates 195 mW.

RM02C-4 11:10 Room: HCC-316B
A Low-Power Low-Noise Single-Chip Receiver Front-End for Automotive Radar at 77 GHz in Silicon-Germanium Bipolar Technology

M. Hartmann, C. Wagner*, K. Seemann, J. Platz**, H. Jaeger** ,
R. Weigel, Friedrich Alexander University Erlangen, Germany, * Johannes Kepler University Linz, Austria, ** DICE, Linz, Austria

This paper presents a single chip receiver frontend, including low-noise amplifier and mixer, for application in automotive radar systems at 77 GHz. The circuit has been implemented in a SiGe HBT technology. The front-end shows a minimum measured single sideband noise figure (SSB NF) of 10.5 dB and a maximum conversion gain of 30 dB at 77 GHz. The measured 1 dB compression point of the circuit is -25.5 dBm and the third order intercept point is -21.6dBm at 77 GHz.

RM02C-5 11:30 Room: HCC-316B
80-GHz/160-GHz Transceiver in SiGe HBT Technology

E. Laskin, P. Chevalier*, A. Chantre*, B. Sautreuil*, S. P. Voinigescu,
University of Toronto, *STMicroelectronics

A single-chip, mm-wave transceiver, transmitting and receiving simultaneously at 80/160-GHz bands, is fabricated in SiGe HBT technology. The circuit features an 80-GHz quadrature Colpitts oscillator with differential outputs at 160GHz, a double-balanced Gilbert-cell mixer, and two broadband 70-270GHz stacked transformers. The downconversion gain is -20.5dB for RF inputs between 70-94GHz and -23.5dB for inputs in the 150-170GHz band. The oscillator generates +5.5dBm at 80GHz and -7dBm at 160GHz.

Monday June 4, 2007

10:10

Room: HCC - 316A

Session RM02D: Device Technology

Chair: Aditya Gupta, ANADIGICS

Co-Chair: Chang-Ho Lee, Samsung

RM02D-1 10:10

Room: HCC-316A

INVITED: The Present State of the Art of Wide-Bandgap Semiconductors and Their Future

M. J. Rosker, Defense Advanced Research Projects Agency (DARPA)

This paper summarizes recent improvements in the performance and reliability of microwave and millimeter-wave wide-bandgap gallium nitride on silicon carbide devices and their promise for future integrated circuits. Many recent advances have been made as a result of the on-going Phase II Wide Band Gap Semiconductor for RF Applications (WBGs-RF) program funded by the Defense Advanced Research Projects Agency (DARPA).

RM02D-2 10:30

Room: HCC-316A

Experimental Study on the Role of Hot Carrier Induced Damage on High frequency Noise in Deep Submicron NMOSFETs

H. Su, H. Wang, T. Xu, R. Zeng, Nanyang Technological University, Singapore

Impact of hot carrier induced interface damage and its spatial location on RF noise in NMOSFETs is studied. The increase in N_{Fmin} and R_n after hot carrier stress cannot be simply explained by the change of the inversion carrier density. It was demonstrated that the presence of interface states at source side shows much greater impact on the degradation of N_{Fmin} and R_n . This provides strong experimental evidence for the source-side dominant spatial origin of channel noise.

RM02D-3 10:50 Room: HCC-316A
**High-Q Integrated Inductor Using Post-CMOS
Selective Grown Porous Silicon (SGPS) Technique for
RFIC Applications**

C. Li, H. Liao, C. Wang, J. Yin, R. Huang, Institute of Microelectronics,
Peking University

This paper reports a new category of high-Q integrated inductor realized using post-CMOS selective grown porous silicon (SGPS) technique. The SGPS technique can effectively reduce substrate loss. The inductors are fabricated in standard RF CMOS process firstly and then Q-factors are improved through SGPS technique. For a 2.1nH inductor, a 105% increase (from 9.5 to 19.4) in peak Q is obtained. A 2.45 GHz VCO using SGPS inductor achieves 7.2dBc phase noise improvement at 100 kHz frequency offset.

RM02D-4 11:10 Room: HCC-316A
**Characterization and Modeling of Metal/Double-
Insulator/Metal Diodes**

S. Rockwell, D. Lim, B. Bosco, J. Baker, B. Eliasson*, M. Forsyth*,
M. Cromar*, Motorola Labs, *Phiar Corp

In this paper we present measurements, models, and circuit implementations for a new low cost, thin film, metal - double-insulator - metal (MIIM) based tunneling diode technology. The device technology uses two insulators to form a tunneling device with very high speed performance capability, and potentially compatible with many substrate technologies.

RM02D-5 11:30 Room: HCC-316A
Fully Depleted SOI RF Switch with Dynamic Basing

C. L. Chen, C. K. Chen, P. W. Wyatt, J. M. Knecht, D.-R. Yost, P. M. Gouker,
P. D. Healey, and C. L. Keast, MIT Lincoln Laboratory

RF switches in FDSOI are reported for the first time. In a novel biasing circuit, the conventional bias resistor is replaced with an FET, which functions as a variable resistor and presents optimal resistance for the on- and off-state. The low capacitance of FDSOI improved the switch performance and the dynamic biasing further increased saturated power. At 5 GHz, a fully integrated SPDT switch has 0.75-dB of insertion loss, 39-dB of isolation, and 1-dB compression power approaching 33 dBm.

Monday June 4, 2007

13:20

Room: HCC - 313A

Session RM03A: 3G and SDR

Chair: Didier Belot, ST Microelectronics

Co-Chair: Andre Hanke, Infineon

RM03A-1 13:20

Room: HCC-313A

INVITED: Digital RF Processor (DRP) for Mobile Phones

R. B. Staszewski, K. Muhammad, and O. Eliezer, Texas Instruments

RF circuits for wireless applications have recently migrated to low-cost digital nanoscale CMOS processes, which are optimized for digital logic and SRAM memory and are extremely unfriendly for conventional analog and RF designs. We present fundamental techniques that transform the RF and analog circuit design complexity to digital domain for a wireless RF transceiver. The ideas presented have been used in Texas Instruments to develop commercial single-chip Bluetooth and GSM radios.

RM03A-2 13:40

Room: HCC-313A

Analog Path for Triple Band WCDMA Polar Modulated Transmitter in 90nm CMOS

S.Akhtar, P. Litmanen, M. Ipek, J. (H.-C.) Lin*, S. Pennisi, F.-J.Huang ,
R. B. Staszewski, Texas Instruments, Inc., *Now with MStar
Communications

We present a fully integrated analog path for a 3G polar transmitter in 90nm CMOS. It includes a quad band Digitally Controlled Oscillator providing modulation for the phase data and a single stage Digital Pre-Power Amplifier that combines the phase and amplitude signals while providing the dynamic range for WCDMA. The chip, with integrated LDOs, consumes 60mA from a 1.4V supply while providing 11dBm CW power at 1950MHz, 87dB dynamic range without any calibration, and PN of -157dBc/Hz at 40MHz.

RM03A-3 14:00 Room: HCC-313A

A 100 MHz – 2.5 GHz Direct Conversion CMOS

Transceiver for SDR Applications

G. Cafaro, T. Gradishar, J. Heck, S. Machan, G. Nagaraj, S. Olson, R. Salvi, B. Stengel, B. Ziemer, Motorola Labs

This paper describes a fundamentally flexible transceiver implemented in 90 nm CMOS. Flexible programming allows the RFIC to process signals of multiple wireless protocols from 100 MHz – 2.5 GHz with channel bandwidths from 8 KHz to 20 MHz. At 1.8 GHz the receiver noise figure is 7 dB with IP₃ of –6 dBm and voltage gain of 48 dB. The transmitter has better than 40 dB carrier suppression and EVM of 1% at 800 MHz. Direct digital synthesizers provide independent LO signals for transmit and receive.

RM03A-4 14:20 Room: HCC-313A

A Wideband OFDM Transceiver Implementation for Beyond 3G Radio Systems

J.S.Koskinen, P.T.Eloranta, P.Seppinen, P.Kosonen, A.Pärssinen, Nokia Research Center

The implemented ASICs, intended for mobile terminal usage, comprise a wideband high capacity OFDM direct conversion transceiver front-end for beyond 3G cellular systems. The transceiver operates with 83.2 MHz signal bandwidth and is designed for the operational frequency range of 5.15-5.725 GHz. The receiver and transmitter chips were fabricated with 0.13 μ m BiCMOS technology.

RM03A-5 14:40 Room: HCC-313A

A Disruptive Software-Defined Radio Receiver Architecture Based on Sampled Analog Signal Processing

F. Rivet*, Y. Deval*, J-B. Begueret*, D. Dallet*, D. Belot**,
*IXL Laboratory, University of Bordeaux, Talence, France,
**ST Microelectronics, Central R&D, Crolles, France

Software Defined Radio (SDR) aims at bringing digital treatment chip closer to the antenna in a mobile terminal architecture. The main goal is to create a reconfigurable radio architecture accepting all the cellular or non-cellular standards working in the 0-5 GHz frequency range. The idea is to interface a preprocessing circuit between the antenna and a Digital Signal Processor (DSP) to pre-condition the RF signal. This paper presents the design of an analog discrete-time device.

Monday June 4, 2007

13:20

Room: HCC - 313B

Session RM03B: Techniques for WiMedia UWB

Chair: Stefan Heinen, Infineon Technologies AG

Co-Chair: Jacques C. Rudell, Intel Corp.

RM03B-1 13:20 Room: HCC-313B

INVITED: Low-Cost Direct Conversion RF Front-Ends

J.-H. C. Zhan, B. R. Carlton* and S. S. Taylor*, MediaTek, Intel*

This paper reviews architectures and circuit techniques suitable for highly integrated broadband receiver front-ends. Direct conversion simplifies the receiver architecture, resistive feedback LNAs reduce silicon area and current mode passive mixer operation improves the receiver linearity and reduces flicker noise. A 2-5.8GHz receiver front-end dissipating 85mW at 5GHz while occupying 0.2 mm² active area is fabricated as a demonstration of the combination of these concepts.

RM03B-2 13:40 Room: HCC-313B

3.1-4.7GHz WiMedia UWB RF/Analog Front-End in 130nm CMOS

M.W. Lynch*, C. Demirdag*, N. Belabbes*, S. Carnevali*, C. Lacy*, M. Yu*, W. An*, H. Jin*, J. Park**, D.S. Malhi*, *Synopsys, Mississauga, ON, Canada **SiTrix, Woburn, MA

A highly integrated transceiver for WiMedia UWB applications is presented. Implemented in 130nm CMOS and operating from 1.2V and 2.5V supplies, it features direct conversion transmit and receive paths. Three PLLs with ring-oscillator VCOs are used in a fast-hopping (~2ns) frequency synthesizer. On-chip calibration is used by several blocks for I/Q mismatch, filter tuning, DC offset cancellation and power control. The transceiver achieves a Tx EVM better than -20.6dB when operated in 480Mbps.

RM03B-3 14:00 Room: HCC-313B

A Dual-Band Direct-Conversion RF Front-End for WiMedia UWB Receiver

J. Kaukokuuori, J. Ryyänen, K. A. I. Halonen, Helsinki University of Technology, Electronic Circuit Design Laboratory

A direct-conversion RF front-end designed for BG1 and BG3 WiMedia UWB receiver is described. It includes multi-stage LNAs, down-conversion mixers, a polyphase filter, and local oscillator buffers. The front-end achieves approximately 26-dB gain and 4.9 to 5.6-dB noise figure (NF) across three subbands of BG1. In BG3 it obtains 23 - 26-dB gain and 6.9 to 7.7-dB NF. It consumes 48.1 mA and 42.7 mA from a 1.2-V supply voltage in BG1 and BG3, respectively. The chip was implemented in a 0.13- μm CMOS.

RM03B-4 14:20 Room: HCC-313B

A 0.18- μm CMOS Low-spurious Local Signal Generator for MB-OFDM UWB Radio

T. Tokairin, N. Matsuno, K. Numata, T. Maeda, S. Tanaka, NEC Corporation

This paper presents a new single PLL and single SSB-mixer architecture for a local signal generator of the Mode-1 MB-OFDM UWB systems. By introducing a VCO running at 8976 MHz and a divide-by-8.5/17 circuit using double-edge triggered operation, three bad carrier signals with low spurious levels, which are required in Japan and Europe, can be obtained. A fabricated 0.18- μm CMOS local signal generator has below -41 dBc spurious levels for band #3 carrier with a small core area of 0.67 mm².

RM03B-5 14:40 Room: HCC-313B

A Cochlea-based Preselector for UWB Applications

C. Galbraith, G. M. Rebeiz*, R. Drangmeister**, The University of Michigan, *University of California, San Diego, **M.I.T. Lincoln Laboratory

A compact, contiguous-channel multiplexer has been developed using a silicon multi-chip module (MCM) process. The passive channelizing filter is based on the mammalian cochlear response, covers 2-7 GHz in 15 channels (16% bandwidth) and occupies an area of 48 square mm. Such a filter finds application in integrated wideband and ultra-wideband (UWB) systems as a receiver preselector filter and/or a spectrum activity monitor.

Monday June 4, 2007

13:20

Room: HCC - 316B

**Session RM03C: Advanced Frequency Synthesis
Techniques**

Chair: B. Bakkaloglu, Arizona State University

Co-Chair: Ting-ping Liu, Winbond Electronics

RM03C-1 13:20 Room: HCC-316B

**INVITED: Single and Dual Loop Ring Oscillator Based
Frequency Synthesizers for Broadband Tuner
Applications**

A. Maxim, Silicon Laboratories Inc., Austin, TX

Two low phase noise and low spur level ring oscillator synthesizers, compatible with the demanding DVB-S satellite and DVB-T/C terrestrial and cable TV applications. A DVB-S single-loop 0.9-2.2GHz integer-N PLL using a fully-integrated noise attenuator loop filter, achieving a $<1.3^\circ$ rms double sided integrated phase noise and <-50 dBc spurs. A DVB-T/C dual-PLL 70-950MHz integer-N synthesizer using a sample and hold discrete loop filter, achieving <-80 dBc spurs and $<0.7^\circ$ integrated phase noise.

RM03C-2 13:40 Room: HCC-316B

**Frequency Synthesizer and FSK Modulator for IEEE
802.15.4 Based Applications**

W. Rahajandraibe, L. Zaid, V. Cheynet de Beaupré, G. Bas*, L2MP -
University of Provence, FRANCE, *STMicroelectronics, FRANCE

The feasibility of a low cost, 2.5 Volts supply phase-locked loop for HomeRF application is demonstrated. Based on IEEE 802.15.4 specification, this PLL is used in a STMicroelectronics proprietary system to achieve both frequency synthesis and frequency shift keying (FSK) modulation. Simulation results of the PLL and the open loop modulation together with VCO measurements are presented. All the circuits have been fully integrated using STMicroelectronics 0.28 μ m CMOS technology.

RM03C-3 14:00 Room: HCC-316B
A 9.1-to-11.5-GHz Four-Band PLL for Ku-Band Satellite & Optical Communication Applications

J.-Y. Lee, K. Kim, S.-C. Lee, J.-K. Kwon, J. Kim, S.-H. Lee, Electronics & Telecommunications Research Institute

In this paper, we present the 4-band PLL of 9.1 to 11.5 GHz. In the proposed PLL, both improved multi-modulus divider and adaptive 4-band LC VCO are depicted. The multi-modulus divider provides division ratios of 6 to 455 depending on the division mode of the six-mode prescaler. The LC VCO generates 9.1 GHz to 11.6 GHz, including adaptive cross-coupled MOS array. The cross-coupled MOS array is devised to reduce the area of capacitor array and provide additional power.

RM03C-4 14:20 Room: HCC-316B
A Fully On-Chip 10Gb/s CDR in a Standard 0.18 μ m CMOS Technology

J. Li and J. Silva-Martinez, Texas A&M University, Analog and Mixed-Signal Center

A fully integrated OC-192 clock-data recovery (CDR) architecture in standard 0.18 μ m CMOS is described. The CDR integrates the large filter and satisfies SONET jitter tolerance requirements with a total power dissipation (including the buffers) of 290mW. The measured RMS jitter of the recovered data is 0.74ps with a bit-error rate (BER) less than 10⁻¹² when the input PRBS data pattern has a pattern length of 2¹⁵-1 and a total horizontal eye closure of 0.54 U_{lpp} due to the added ISI distortion.

RM03C-5 14:40 Room: HCC-316B
A 9-Bit 9.6GHz 1.9W Direct Digital Synthesizer RFIC Implemented In 0.18micron SiGe BiCMOS Technology

X. Yu*, F. F. Dai*, **D. Yang*, V. Kakani*, J. D. Irwin*, R. C. Jaeger*,
*Auburn University, **Amtec Corporation

This paper presents a low power SiGe DDS MMIC with 9-bit phase and 8-bit amplitude resolutions. Using more than 9600 transistors, the active area of the DDS is 2.3x0.7mm². The maximum clock frequency was measured at 9.6GHz with 4.8GHz Nyquist output and 1.9W power consumption under 3.3V/4.0V dual power supplies. The DDS achieves the best reported power efficiency figure of merit of 5.1 GHz/W. The measured SFDR is 30dBc with 2.4GHz outputs at clock frequency of 9.6GHz.

Monday June 4, 2007

13:20

Room: HCC - 316A

Session RM03D: Transmitter Linearization Techniques

Chair: Freek van Straten, NXP Semiconductor

Co-Chair: Joe Staudinger, Freescale Semiconductor

RM03D-1 13:20 Room: HCC-316A

INVITED: Application of Digital Adaptive Pre-distortion to Mobile Wireless Devices

G. Norris, J. Staudinger, J.-H. Chen, C. Rey, P. Pratt, R. Sherman, H. Frazz*, Freescale Semiconductor, *Georgia Tech

Low power adaptive pre-distortion (APD) techniques are applied to nonlinear RF power amplifiers for mobile devices. An APD system is demonstrated which reduces spectral regrowth products by 10-20dB and increases modulation accuracy by 2-6X. The use of PD allows a reduction in 3G PA supply current by 2X and provides immunity to load mismatches as high as 8:1.

RM03D-2 13:40 Room: HCC-316A

A High Performance Balanced Power Amplifier and its Integration into a Front-end Module at PCS Band

G. Zhang, S. Chang, Z. Alon, Skyworks Solutions Inc.

A novel load insensitive power amplifier (LIPA) with balanced structure is developed for 3G handset application at PCS band. No external regulated voltage and analog voltage supplies are required at high power level and it is compatible with DC-to-DC converter. Digital or analog control may be applied to further improve its PAE at low and middle power levels. This newly featured PA is integrated into a $4 \times 7 \text{mm}^2$ front-end module (FEM) with good performance, especially under load mismatch condition.

RM03D-3 14:00 Room: HCC-316A

Power Amplifier Predistortion Linearization Using a CMOS Polynomial Generator

A.A.Kidwai, Intel Corporation

In this work, an Analog Predistortion chip has been developed in $0.18 \mu\text{m}$ CMOS technology and tested in the lab. Linearity improvement of 6-7 dB for Power Amplifiers has been demonstrated over 60MHz bandwidth. The chip has also been tested to linearize externally modulated fiber-optic links and SFDR improvement of 8dB was achieved for a bandwidth of 40MHz.

RM03D-4 14:20 Room: HCC-316A
Switched Doherty Power Amplifiers for CDMA and WCDMA

T. R. Apel, Y. Tang, O. Berger, Triquint Semiconductor, Inc.

Power amplifiers for CDMA and WCDMA applications must provide competitive power efficiency at low power levels as well as at full power. This paper presents a novel approach that utilizes a modified Doherty architecture as a solution to this problem. PACs in both cellular and PCS bands are presented. Typical performance is -50dBc ACPR at PAE levels of 40% in high power mode (+28dBm) and 21% in low power mode (+16.5 dBm). Design methodology, new HBT cell geometry and manifold are also discussed.

RM03D-5 14:40 Room: HCC-316A
A 2.4GHz Fully Integrated Transmitter Front End with +26.5-dBm On-Chip CMOS Power Amplifier

P.C. Wang, C.J. Chang, W.M. Chiu, P.J. Chiu, C.C. Wang, C.H. Lu, K.T. Chen, M.C. Huang, Y.M. Chang, S.M. Lin, K.U. Chan, Y.H. Lin, C.C. Lee, Realtek Semiconductor Corp.

A fully integrated transmitter front end with on-chip power amplifier (PA) in 0.18um CMOS technology is presented. The on-chip PA employs dynamic bias technique to reduce power consumption and enhance linearity. In the measurement, it reveals the output 1dB of the PA is 26.5dBm. Also, the transmitter delivers an average power of 17.3dBm with EVM of -28.1 while drawing 225mA of DC current (PA 157mA) from 3.3V supply. The low power consumption, adequate linearity and high integration make this transmitter suitable for WLAN application.

Monday June 4, 2007

15:30

Room: HCC - 313A

Session RM04A: RFID

Chair: Natallino Camilleri, Alien Technology

Co-Chair: Srenik Mehta, Atheros Communications

RM04A-1 15:30 Room: HCC-313A

An 860 to 960MHz RFID Reader IC in CMOS

P. B. Khannur, X. Chen, D. L. Yan, D. Shen, B. Zhao, M. K. Raja, Y. Wu
A. B. Ajikuttira, W. G. Yeoh, R. Singh, Institute of Microelectronics,
Singapore

A UHF RFID Reader IC in 0.18 μ m CMOS covering the entire 860MHz to 960MHz RFID band is presented in this paper. The IC meets the EPC Class-1 Generation-2 and ISO-18000 standards. The transmitter output is +10dBm and the receiver sensitivity is -96dBm in listen-before-talk mode (LBT) and -85dBm in talk-mode (TM). The IC contains 10-bit DACs, pulse-shaping filters, IQ Modulator and Power amplifier in transmit chain and receive front-end with IQ down converter, channel-select filters with Variable-gain amplifiers and 10-bit ADCs. The frequency resolution of 50kHz is achieved with the on-chip Dual-loop synthesizer with phase noise of -101dBc/Hz at 100kHz offset. The chip incorporates ASK demodulators. The chip has a die area of 6mm X 6mm and draws 300mA current from 1.8V supply and operates over a temperature range from -25°C to +75°C.

RM04A-2 15:50 Room: HCC-313A

A UHF Mobile RFID Reader IC with Self-Leakage Cancellation

J.Y. Lee, J.H. Choi, K.H. Lee, B.K. Kim, M.S. Jeong, Y.H. Cho, H.Y. Yoo,
K.O. Yang, S.Y. Kim, S.M. Moon, J.Y. Lee, S.K. Park, W.C. Kong, J. Kim,
T.J. Lee, B. E. Kim, B.K.Ko, Analog Devices, Inc.

Developed UHF mobile single chip RFID reader achieves DA output power of 3 dBm, OIP₃ of 14.8 dBm, phase noise of -100 dBc/Hz at 100 kHz offset, noise figure of 35.5 dB for talk mode, 6.2 dB for listen before talk(LBT) mode, and current consumption of 108mA from a 1.8 V supply. A leakage signal cancellation scheme is employed to suppress inevitable Tx leakage into Rx input. At a distance of 90 cm between antenna and tag, the average recognition ratio is increased from 0% to 42.8% by this scheme.

RM04A-3 16:10 Room: HCC-313A
A 900-MHz Direct-Conversion Transceiver for Mobile RFID Systems

J. Jang, H. Lee, S. W. Choi, K. Ahn, M. S. Jung, E. S. Song, J. Kim, H. H. Roh, G. B. Kim, S. W. Bae, H. R. Oh, Y. R. Seong, J. S. Park, U-Comm Technology Co. Ltd., School of Electrical Engineering, Kookmin University, Seoul

A Fully integrated 900-MHz Direct-Conversion transceiver for mobile RFID system is presented. The transceiver consists of a low noise amplifier, a down-conversion mixer, a band pass filter, and programmable gain amplifier (PGA) for RX path; and a power amplifier, an up-conversion mixer, a low-pass filter, and a PGA for TX path. In addition, the fractional N PLL is integrated to cover different frequency standards for different nations.

RM04A-4 16:30 Room: HCC-313A
Development of Long-Range UHF-band RFID Tag Chip Using Schottky Diodes in Standard CMOS Technology

N. Tran, B. Lee, J. -W. Lee, School of Electronics and Information, Kyung Hee University, Korea

We present the design of building blocks for UHF-band passive RFID tag chip, i.e., voltage multiplier, ASK demodulator, and internal clock generator. The Schottky diodes used in the passive RFID tag chip were fabricated using Titanium -Silicon junction $0.35\ \mu\text{m}$ CMOS process. For 300 mV RF input voltage, the fabricated voltage multiplier using Schottky diodes generated output voltages of 1.5 V and corresponding voltage conversion efficiency of 45%.

RM04A-5 16:50 Room: HCC-313A
An RFID System with Fully Integrated Transponder

A. Shameli, A. Safarian, A. Rofougaran*, M. Rofougaran*, F. De Flaviis, University of California at Irvine, *Broadcom Corporation

This paper presents an RFID system with fully integrated transponder. The transmit path of the reader as well as key blocks of the tag is designed and fabricated in standard CMOS $0.18\ \mu\text{m}$ process. The system operates at 900MHz with the coverage range of more than 0.5cm. The tag's antenna is integrated on chip without using any special process. The reader employs a coil switching technique to increase its coverage area.

Monday June 4, 2007

15:30

Room: HCC - 313B

Session RM04B: Advanced Interconnect and Pad Modeling

Chair: Francis Rotella, Fujitsu Laboratories of America

Co-Chair: Louis Liu, Northrup Grumman

RM04B-1 15:30 Room: HCC-313B

A Wideband Scalable and SPICE-Compatible Model for On-Chip Interconnects Up To 80 GHz

K. Kang^{**}, L. Nan^{**}, S. C. Rustagi^{*}, K. Mouthaan^{**}, J. Shi^{*},
R. Kumar^{*} and L.-W. Li^{**}, ^{*}Institute of Microelectronics, Singapore
117685; ^{**}Department of Electrical & Computer Engineering, National
University of Singapore, Singapore.

A fully scalable and SPICE compatible wide band model up to 80 GHz of on-chip interconnects is presented in this paper. The values of frequency-independent elements of the proposed model are determined by analytical techniques. The model is validated by both full-wave simulation and measurements. The simulated S-parameters of the model agree well with the measured S-parameters of on-chip interconnects with different widths and lengths over a wide frequency band from DC up to 80 GHz.

RM04B-2 15:50 Room: HCC-313B

CPW and Discontinuities Modeling for Circuit Design up to 110 GHz in SOI CMOS Technology.

A.Siligaris, C.Mounet, B.Reig, P. Vincent, CEA/LETI-MINATEC,
Grenoble France

This paper presents models for CPW and CPW discontinuities implemented in SOI CMOS technology. Empirical equations, are used to describe the electrical behavior of CPW as a function of the line's geometrical parameters. The models are validated through measurements up to 110 GHz. Thanks to accurate full wave simulations, discontinuities are improved, and electrical models are developed. Finally, a 60 GHz band-pass filter is designed and the simulations are compared to measurements.

RM04B-3 16:10 Room: HCC-313B

A Scalable Lossy Substrate Model for Nanoscale RF MOSFET Noise Extraction and Simulation Adapted to Various Pad Structures

J. C. Guo, Y. H. Tsai, Dept. of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

A broadband and scalable lossy substrate model is developed and validated for nanoscale RF MOSFETs of different finger numbers and adopting various pad structures such as lossy, normal, and small pads. The broadband accuracy is justified by good match with S- and Y-parameters up to 40 GHz. The measured noise characteristics in terms of four noise parameters can be accurately simulated up to 18 GHz. The scalable lossy substrate model can consistently predict the abnormally strong finger number dependence and nonlinear frequency response of noise figure (NF_{min}) revealed by devices with lossy pads. Furthermore, the scalable model can precisely distribute the substrate loss between the transmission line (TML) and pads of various metal topologies and the resulted excess noises. The enhanced model provides useful guideline for appropriate layout of pads and TML to effectively reduce the excess noise. The remarkably suppressed noise figure to ideally intrinsic value can be approached by small pad in this paper.

RM04B-4 16:30 Room: HCC-313B
Ultra Low-Capacitance Bond Pad for RF Applications in CMOS Technology

Y.-W. Hsiao, M.-D. Ker, Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University

A low-capacitance bond pad for gigahertz RF applications is proposed. Three kinds of on-chip inductors embedded under the traditional bond pad are used to compensate bond-pad capacitance. Experimental results have verified that bond-pad capacitance can be significantly reduced in a specific frequency band due to the cancellation effect provided by the embedded inductor in the proposed bond pad. The proposed bond pad is fully compatible to general CMOS processes without any process modification.

RM04B-5 16:50 Room: HCC-313B
Experimental Characterization of the Effect of Metal Dummies on Spiral Inductors

L. Nan*, K. Mouthaan*, Yong-Zhong Xiong**, Jinglin Shi**, S. C. Rustagi** and B.-L. Ooi*, *Department of Electrical and Computer Engineering, National University of Singapore, Singapore, **Institute of Microelectronics, Singapore

In modern CMOS technologies, metal dummies are required to maintain metal density uniformity and to planarize the layers. As frequency increases, the effect of the metal dummies on the CMOS integrated circuits or components should be taken into account. This work presents experimental results of the effect of metal dummies on the Q-factor and the equivalent model parameters of the spiral inductors fabricated in a standard 0.18- μm CMOS technology up to 40 GHz.

Monday June 4, 2007

15:30

Room: HCC - 316B

Session RM04C: Advanced Front-End Circuits

Chair: Sayfe Kiaei, Arizona State University

Co-Chair: Walid Ali-Ahmad, American University of Beirut

RM04C-1 15:30 Room: HCC-316B
Asymmetric DC Offsets and IIP2 in the Presence of LO Leakage in a Wireless Receiver

I. Elahi, K. Muhammad, Texas Instruments Inc.

We present mathematical analysis to prove that LO leakage at the input of RF circuits in the presence of finite IIP3 results in asymmetry in DC offsets and IIP2 between in-phase and quadrature channels in a wireless receiver. The asymmetry in IIP2 causes effective IIP2 of the receiver to be at best only 3dB higher than the smaller of two IIP2 values. Measurement data from a quad-band GSM/GPRS receiver implemented in 90-nm digital CMOS process is also presented to support mathematical analysis.

RM04C-2 15:50 Room: HCC-316B
A Low-Noise 2.5GHz Direct-Conversion Receiver Front-End With Low-Distortion Baseband Filters

O. Shana'a, Maxim Integrated Products

A 2.5GHz direct conversion receiver front-end has a 3.2dB DSB NF, -14dBm IIP3, and +27dBm IIP2, referred to the LNA input. The RF I/Q mixers are configured as Gm-cells interfacing to current-mode CMOS I/Q continuous-time Elliptic filters. The filters can operate from a 1V supply and achieve an average input noise current of 11.2 pA/sqrt(Hz), <3% tuning accuracy and <0.5% I/Q bandwidth matching. The receiver draws 30mA from a 2.7 V supply. The chip is fabricated in a 0.5u 46GHz fT BiCMOS process.

RM04C-3 16:10 Room: HCC-316B
A CMOS 5GHz Image-Reject Receiver Front-End Architecture

D. Ozis, J. Paramesh, D. J. Allstot, University of Washington, Seattle, WA, 98195, Telegents Systems, Inc., Sunnyvale, CA 94085, Carnegie Mellon University, Pittsburgh, PA

A fully-integrated double quadrature heterodyne receiver front-end uses a two-stage Lange coupler and achieves a measured image rejection ratio > 55 dB over a 200MHz bandwidth at 5.25 GHz without any tuning or trimming. It also features 23.5 dB gain, -79dBm sensitivity, 5.6 dB SSB noise figure, -7 dBm IIP3, -18dB S11 and 1mm x 2mm chip area in 0.18 μ m CMOS

RM04C-4 16:30 Room: HCC-316B
A 500microW 2.4GHz CMOS Subthreshold Mixer for Ultra Low Power Applications

H. Lee, S. Mohammadi, Purdue University

This paper presents an integrated 2.4GHz ultra low power CMOS down-converting active mixer where all MOS transistors are optimally biased in subthreshold region. At only 500uW DC power consumption under 1.0V supply voltage and small LO power of -9dBm, this mixer has a measured conversion gain of 15.7dB, DSB noise figure of 18.3dB, IIP₃ of -9dBm and 33dB LO to RF isolation. With a help of newly defined figure of merit, this mixer is superior to conventional CMOS mixers reported in the literature.

RM04C-5 16:50 Room: HCC-316B
A 2.5mW 900MHz Receiver Employing Multiband Feedback with Bias Current Reuse

J. Han, R. Gharpurey, University of Texas at Austin

A down-conversion receiver that employs a merged IF-amplifier and mixer is described. Down-converted signal at IF is fed back into the mixer transconductor for further amplification. The receiver operates at a nominal supply voltage of 1.2 V with a current requirement of 2.1 mA and provides a peak conversion-gain of 55 dB. The SSB noise figure is 13 dB at an IF of 1 MHz and 9.8 dB at an IF of 4 MHz. The receiver is implemented in a 0.13- μ m CMOS process, with a core area of less than 0.1 mm².

Monday June 4, 2007

15:30

Room: HCC - 316A

Session RM04D: Advanced Testing Techniques

Chair: Adiyta Gupta, ANADIGICS

Co-Chair: Danilo Manstretta, Universita' degli Studi di Pavia

RM04D-1 15:30 Room: HCC-316A

**INVITED: Built-in Self Test of RF Transceiver SoCs:
From Signal Chain to RF Synthesizers**

A. Valdes-Garcia, W. Khalil* , B. Bakkaloglu** , J. Silva-Martinez*** ,
E. Sanchez-Sinencio***, IBM Research, Intel Corporation* , Arizona State
University**, Texas A&M University***

Built-in self test techniques for local oscillator phase noise, RF front-end circuits, baseband building blocks and transceiver loop-back are described. CMOS implementation of integrated RF test components, including RF detectors and phase discriminators are introduced. These devices eliminate the need for expensive external test equipment. These test strategies can also be used at wafer-level for fault detection/localization. Silicon measurement results verifying these techniques are provided.

RM04D-2 15:50 Room: HCC-316A

Built-in Self Testing of a DRP-Based GSM Transmitter

O. Eliezer, I. Bashir, R. B. Staszewski, and P. T. Balsara* , Texas
Instruments, *University of Texas at Dallas

A novel approach for built-in self-testing of an RF wireless transmitter. It is based on fully-digital hardware and on software algorithms and allows testing of the transmitter's RF circuitry while providing low-cost replacements for the costly traditional RF tests. The testing approach is structural in nature and substitutes for the high-cost test equipment and extended test times. The techniques have been successfully verified in a commercial single-chip GSM radio in 90-nm CMOS.

RM04D-3 16:10 Room: HCC-316A
A Sub 1V CMOS LNA Dedicated to 802.11b/g Applications with Self-test & High Reliability Capabilities.

M. Cimino, M. De Matos, H. Lapuyade, T. Taris, Y. Deval & J. B. Bégueret, IXL Laboratory, University of Bordeaux1

A Low Noise Amplifier designed in a 0.13 μ m CMOS technology, which has self-test and high reliability capabilities, is presented. Such a LNA could be used in the design of front-end of critical WLAN nodes to ensure the data transmission. The test is based on a Built-In Self Test methodology to monitor the LNA's behavior and the LNA's reliability is ensured by the use of redundancies. The LNA works under a 0.9V supply voltage and the test chip has characteristics suitable for 802.11b/g applications.

RM04D-4 16:30 Room: HCC-316A
On-Chip Circuit for Measuring Data Jitter in the Time or Frequency Domain

M. Ishida, K. Ichiyama, T.J. Yamaguchi, M. Soma*, M. Suda**, T. Okayasu**, Advantest Laboratories, Ltd., *University of Washington, **Advantest Corporation

An on-chip data jitter measurement circuit in 0.11- μ m CMOS is demonstrated. It utilizes a data-to-clock converter, pulse generators, and an integrator followed by a sample-&-hold. The circuit outputs a data jitter waveform in real-time, and doesn't require a reference clock. Its measurement linearity is 11 uV/ps with an error of 1.56 ps-RMS for a 2.5 Gbps 7-stage PRBS.

RM04D-5 16:50 Room: HCC-316A
Direct Extraction Techniques for Thermal Resistance of MESFET and HEMT Devices.

I. Angelov, C. Kärnfelt, Chalmers University of Technology, Sweden

A simple technique for direct extraction of junction temperature and thermal resistance for MESFET and HEMT FET is proposed and experimentally evaluated. The techniques were applied for thermal resistance extraction of the mHEMT devices in a microstrip tree-stage amplifier before and after flip chip assembly.

Tuesday June 5, 2007

08:00

Room: HCC - 313A

Session RTU1A: Wireless LAN Transceivers

Chair: Glenn Chang, Maxlinear

Co-Chair: Srenik Mehta, Atheros Communications

RTU1A-1

08:00

Room: HCC-313A

An Area and Power Efficient Cartesian Phase Shifter + Mixer Circuit Applied to WLAN System

A. Afsahi*, A. Behzad*, S. Au*, R. Roufoogaran**, J Rael**, *Broadcom Corp, San Diego, **Broadcom Corp, Irvine

A two-antenna array receiver is designed for WLAN application to build a maximum ratio combiner (MRC) system. A new signal-path Cartesian phase generation and combination technique is proposed to shift the RF signal by 22.5 phase steps. The 3dB improvement in received SNR is achieved in comparison to single path receiver. The 0.29mm² RF paths consumes 30mW in 0.13um CMOS process.

RTU1A-2

08:20

Room: HCC-313A

A Low-Power 5GHz Transceiver in 0.13 Micron CMOS For OFDM Applications with Sub-mm² Area

Y. Han, L. E. Larson, University of California, San Diego

A 5GHz direct conversion transceiver is fabricated in a 0.13um CMOS process for WLAN 802.11a applications. The transmitter achieves -56 dBc LO leakage, -36 dBc side-band rejection, -43 dBc 3rd harmonic suppression at 5.4GHz, and an EVM of 3.4% at 5.1GHz with 60mW power consumption. The receiver achieves 3.3 dB NF, 27 dB conversion gain, -14 dBm IIP3, and a measured 1/f noise corner of 110 kHz with 36mW power consumption from a 1.2V supply voltage. The active area was 0.9 mm².

RTU1A-3

08:40

Room: HCC-313A

A Single Chip 802.11abgn Enhancement Mode PHEMT MMIC with dual LNAs, Switches, and Distortion Compensation Power Amplifiers

H.Morkner, M.Vice, M.Karakucuk, W.Abey, L.Nguyen, J.Kessler, R.Ruebusch, Avago Technologies Inc., Wireless Semiconductor Division, San Jose, CA

An enhancement PHEMT MMIC with integrated dual LNAs, Switches, and Linear PAs is presented for use in 802.11abgn FEMs. The dual LNA/switch receivers provide less than 2.4dB and 2.8dB total NF at 16dB gain and 10mA. The dual power amplifiers provide 4% EV/128mA and 6% EVM/167mA at 20dBm power under 54Mbps OFDM 802.11g & a modes. Power down, mode select, and directional power detect are integrated and CMOS compatible. This is the highest integration known to be published for 802.11abgn ASIC.

RTU1A-4 09:00 Room: HCC-313A
A WiMAX Receiver with Variable Bandwidth of 2.5 – 20 MHz and 93 dB Dynamic Gain Range in 0.13-micron CMOS Process

D.-R. Huang, S.-W. Kao, Y.-H. Pang, SoC Technology Center, Industrial Technology Research Institute, HsinChu 310, Taiwan, R.O.C

A low-IF receiver for WiMAX applications has been designed and fabricated in TSMC 1P8M 0.13- μ m CMOS process. It contains a RF front-end and an analog baseband. The programmable gain amplifiers provide 0-65 dB gain range in 1dB step and less than 0.4 dB gain error. The bandwidth of the channel selection filter is reconfigurable from 2.5 MHz to 20 MHz for different requirements in WiMAX applications. The receiver has 4.6 dB noise figure and consumes 50.4 mW with a 1.2 V power supply.

RTU1A-5 09:20 Room: HCC-313A
A Multi-Standard Digital Envelope Modulator for Polar Transmitters in 90nm CMOS.

P.T.M. van Zeijl*, M. Collados**, *Philips Research, **NXP Research

A Multi-Standard Digital Envelope Modulator for a polar transmitter has been designed in a 90nm digital CMOS process for 802.11a/b/g and Bluetooth Medium-Rate. The modulator reaches an output power of 9dBm for 54Mbit/s using 64QAM and fulfilling EVM specifications and spectral mask requirements while consuming 108mW. An output power of 14dBm is reached for 3Mbit/s Bluetooth Medium Rate at 204mW power consumption. Due to 4-phase clocking, envelope aliases are almost completely cancelled.

Tuesday June 5, 2007

08:00

Room: HCC - 313B

**Session RTU1B: High Frequency Wideband
Techniques**

Chair: Madhukar Reddy, Maxlinear

Co-Chair: Ranjit Gharpurey, University of Texas, Austin

RTU1B-1 08:00 Room: HCC-313B

**A 24GHz Pulse-Mode Transmitter for Short-Range
Car Radar**

P. Zhao, H. Veenstra*, J. R. Long**, NXP Semiconductor, *Philips
Research, **Delft University of Technology

A pulse-mode transmitter with low carrier leakage for 24GHz short-range car radar is described. A 12.5dBm output power amplifier, a pulse width and rate control circuit and a voltage reference circuit are included on the IC. The pulse-mode 24GHz output signal is modulated via the final stage bias current to achieve a RF carrier leakage of -50dBm in the off-state. The power dissipation is 360mW when RF is on, 117mW when RF is off, resulting in a typical 122mW dissipation in normal operation.

RTU1B-2 08:20 Room: HCC-313B

**A 0.13micron CMOS Digital Phase Shifter for K-band
Phased Arrays**

K.-J. Koh, G. M. Rebeiz, University of California at San Diego

A 4-bit active digital phase shifter integrated with digital control circuitry in 0.13 μ m CMOS technology is developed for K-band multiple antenna arrays. The phase shifter exhibits 6.6-12.2 deg of rms phase error at 15-26GHz. The average voltage gain ranges from -3.3dB at 15GHz to -1dB at 24GHz. Input P1dB is typically -0.8dBm at 24 GHz with ± 1.5 dBm variations for overall phase states. The core area of the phase shifter is 0.33x0.43mm², with a current consumption of 6.8mA from a 1.5V supply.

RTU1B-3 08:40 Room: HCC-313B
Low Noise Low Cost Rx Solutions for Pulsed 24GHz
Automotive Radar Sensors

S. Pruvost, L. Moquillon, E. Imbs, M. Marchetti, P. Garcia,
STmicroelectronics, FTM Crolles

This paper presents the Low Noise Amplifier and the Gilbert cells zero-IF down-converter integration then the Colpitts Voltage Controlled Oscillator performances of a UWB pulsed radar sensor. The presented topology was used in order to comply with the ETI specifications. Differential topology measurements were discussed. Simulations of the receiver were performed through a whole range of temperature and process variations. Finally, results return the technology abilities for such applications.

RTU1B-4 09:00 Room: HCC-313B
A 52 GHz, 8.5 dB Traveling Wave Amplifier in 0.13 μ m
Standard CMOS Process.

M. Egels, J. Gaubert, P. Pannier, S. Bourdel

The design of a traveling wave amplifier (TWA) in a 0.13 μ m standard CMOS technology is presented. It is designed to maximize the gain-bandwidth product (GBP). Asymmetric cascode, coplanar wave guide (CPW) and losses compensation technique allow to maximize the TWA GBP. Design and modeling of 90 Ω CPW used to synthesize inductors TWA's lines is presented. Simulations with design kit and developed models for CPW show a 52 GHz bandwidth and a 145 GHz GBP.

RTU1B-5 09:20 Room: HCC-313B
A 2-10 GHz Digital CMOS Phase Shifter for
Ultra-Wideband Phased Array System

D.-W.Kang, S.Hong, Korea Advanced Institute of Science & Technology

This paper describes a digital true time-delay phase shifter implemented in 0.18- μ m CMOS process for ultra-wideband phased array application. By employing active switches in the artificial transmission line architecture, the phase shifter exhibits linear phase change versus frequency, digital control, low insertion loss, and reduced circuit size. Shunt-series peaked load increases the bandwidth of the phase shifter, yielding a flat gain response over a wide bandwidth. The fabricated circuit demonstrates a measured 157.5 $^\circ$ phase tuning range in steps of 22.5 $^\circ$ at 10 GHz.

Tuesday June 5, 2007

08:00

Room: HCC - 316B

Session RTU1C: High Performance VCOs

Chair: Stephen Dow, ON Semiconductors

Co-Chair: Yann Deval, IXL Labs

RTU1C-1 08:00 Room: HCC-316B

11.8GHz CMOS VCO With 62% Tuning Range Using Switched Coupled Inductors

M. Demirkan, S. P. Bruss, R. R. Spencer, University of California at Davis

A VCO uses coupled switched inductors to achieve a 61.9% tuning range centered at 11.75GHz. The measured phase noise is -83 and -106dBc/Hz at 100kHz and 1MHz offsets respectively. This 0.076mm² VCO is fabricated in a 90nm standard digital CMOS process, uses 33% more area than a single-inductor VCO and consumes 7.7mW from a 1.2V supply.

RTU1C-2 08:20 Room: HCC-316B

A Colpitts Oscillator Design for a GSM Base Station Synthesizer

J. Steinkamp, F. Henkel, P. Waldow, O. Pettersson*, C. Hedenäs* and B. Medin*, IMST GmbH, Kamp-Lintfort, Germany, *Infineon Technologies AG, Kista, Sweden

This paper presents the design of a VCO using a Colpitts topology. The VCO system is fully integrated and suitable to operate in GSM base station synthesizers. The challenges and requirements for this application will be discussed and the possibility of achieving the performance of the oscillator will be demonstrated. The topology of the VCO core is a varactor tuned Colpitts oscillator which achieves a phase noise of -148 dBc/Hz at 1.8 MHz offset frequency.

RTU1C-3 08:40 Room: HCC-316B
**Temperature Compensated 2.45 GHz Ring Oscillator
with Double Frequency Control**

W. Rahajandraibe, L. Zaïd, V. Cheynet de Beaupré and G. Bas*, L2MP –
University of Provence, IMT Technopole de Chateau Gombert, Marseille,
France, *STMicroelectronics, Rousset, France

A 2.4GHz VCO with double frequency control has been designed using a CMOS 0.28 μ m process for use in frequency synthesizer and open loop FSK modulation circuit in multi-band IEEE 802.15.4 WPAN applications. This double control allows the VCO to maintain its center frequency and tuning range throughout -40°C to 120°C. Measurements show the sensitivity of the VCO center frequency has been reduced from 1300ppm/°C to 73ppm/°C the phase noise is -96dBc/Hz @ 1MHz offset with a power consumption of 18 mW.

RTU1C-4 09:00 Room: HCC-316B
**A Low-Phase-Noise Low-Power 27-GHz SiGe-VCO
Using Merged-Transformer Matching Circuit Technique**

T. Nakamura, T. Masuda, K. Washio, H. Kondoh, Hitachi, Ltd.

A 27-GHz VCO-MMIC, featuring low phase noise of -115 dBc/Hz (at a 1MHz) and large output power of +3.7 dBm with low DC-power dissipation of 111 mW, was developed using a 0.18- μ m SiGe BiCMOS process. A novel merged-transformer matching circuit contributes to reducing the DC-power dissipation keeping a large output power. In our knowledge, the -187-dB figure-of-merit of the VCO-MMIC is the lowest in 30-GHz class VCO fabricated using Si-based technology.

Tuesday June 5, 2007

08:00

Room: HCC - 316A

Session RTU1D: Fully Integrated CMOS PAs

Chair: Noriharu Suematsu, Mitsubishi Electric

Co-Chair: Joe Staudinger, Freescale Semiconductor

RTU1D-1 08:00 Room: HCC-316A

A Monolithic Voltage-Boosting Parallel-Primary Transformer Structures for Fully Integrated CMOS Power Amplifier Design

K. H. An, Y. Kim*, K. S. Yang, H. Kim, W. Woo*, J. J. Chang*, C.-H. Lee*, H. Kim* and J. Laskar, Georgia Institute of Technology, *Samsung RFIC Design Center

A novel monolithic voltage-boosting parallel-primary transformer is presented for the fully integrated CMOS power amplifier design. Multiple primary loops are interweaved in parallel to combine the AC currents from multiple power devices while the higher turn ratio of a secondary loop boosts AC voltages of the combined primary loops at the load of the secondary loop. The proposed interweaved structure is much more compact and separable from power devices, avoiding potential instability.

RTU1D-2 08:20 Room: HCC-316A

A 90nm CMOS Doherty Power Amplifier with Integrated Hybrid Coupler and Impedance Transformer

M. Elmala, R. Bishop, Intel Corporation

An OFDM capable Doherty PA is implemented in 90nm CMOS with integrated quadrature hybrid and impedance transformer. The two amplifiers are optimized to minimize AM-PM distortion. The PA achieves 25dBm Psat using 1.4V supply with 24% PAE, and operates over 1GHz of frequency range centered (from 4GHz to 5GHz). 3dB to 6dB back-off from P1dB is required to achieve -25dB measured EVM across this band, making it suitable for WLAN and WiMAX applications.

RTU1D-3 08:40 Room: HCC-316A
A 2.4Vp-p Output, 0.045-32.5 GHz CMOS
Distributed Amplifier

J. Aguirre, C. Plett, Carleton University

This paper describes a single-ended five-stage CMOS distributed amplifier employing m -derived filter sections in the artificial transmission lines. The distributed amplifier exhibits a measured pass-band gain of 8.8 ± 1 dB for a 5V rail, and a bandwidth of 45 MHz to 29.5 GHz with a unity gain bandwidth of 32.5 GHz. The die size is $0.85 \times 1.0 \text{ mm}^2$. The amplifier exhibits a peak-to-peak output voltage of 2.4 V. This amplifier is suitable for use in communication systems.

RTU1D-4 09:00 Room: HCC-316A
A 5.8 GHz Linear Power Amplifier in a Standard 90nm
CMOS Process using a 1V Power Supply

P.Haldi, D.Chowdhury, G.Liu, A.M.Niknejad, Berkeley Wireless Research Center, Department of EECS, University of California at Berkeley

A fully integrated 5.8 GHz Class AB linear power amplifier (PA) in a standard 90nm CMOS process using thin oxide transistors utilizes a novel on-chip transformer power combining network. The transformer combines the power of four push-pull stages with low insertion loss over the bandwidth of interest and is compatible with standard CMOS process without any additional analog or RF enhancements. With a 1 V power supply, the PA achieves 24.3dBm maximum output power at a peak drain efficiency of 27% and 20.5dBm output power at the 1 dB compression point.

RTU1D-5 09:20 Room: HCC-316A
A 1.8-GHz 2-Watt Fully Integrated CMOS Push-Pull
Parallel-Combined Power Amplifier Design

O. Lee, K. S. Yang, Y. Kim*, H. Kim, J. J. Chang*, W. Woo*, C.-H. Lee* and J. Laskar, Georgia Institute of Technology, *Samsung RFIC Design Center

This paper proposes a parallel-combined CMOS PA design and its analysis. The proposed class-E CMOS PA incorporates with the push-pull parallel-combined power devices and the 1:1:2 (one-turn double primary and two-turn secondary) step-up on-chip transformer. The PA is fully integrated in a standard 0.18- μm CMOS technology without any external balun or matching networks. From the measurements, the output power of 33 dBm and the PAE of more than 30% were achieved with a 3.3-V power supply at 1.8GHz.

Tuesday June 5, 2007

08:00

Room: HCC - 315

Session RTU1E: Passive Components and Techniques

Chair: Eli Reese, Triquint

Co-Chair: Patrick Yue, UC Santa Barbara

RTU1E-1 08:00 Room: HCC-315

A 0.3 Square mm Miniaturized X-Band On-Chip Slot Antenna in 0.13micron CMOS

N. Behdad*, D. Shi, W. Hong, K. Sarabandi, and M. P. Flynn, University of Michigan, Ann Arbor, MI, *University of Central Florida, Orlando, FL

An on-chip miniaturized slot antenna integrated with a CMOS LNA, on the same chip, is presented in this paper. The antenna operates in the 9-10GHz frequency band, occupies a die area of only 0.3mm^2 , and is fabricated in a standard $0.13\mu\text{m}$ RF CMOS process. A LNA implemented on the same substrate is directly matched to the antenna. An efficient shielding technique is used to shield the antenna from the low-resistivity substrate underneath it. Measurement results of the fabricated prototype indicate that the antenna shows an active gain of -4.4 dBi and an efficiency of 9% in spite of its close proximity to the lossy silicon substrate.

RTU1E-2 08:20 Room: HCC-315

A 60-GHz Millimeter-wave CMOS Marchand Balun

J.-X. Liu, C.-Y. Hsu, H.-R. Chuang, C.-Y. Chen*, Institute of Computer and Communication Engineering, Dept. of Electronic Engineering, National Cheng Kung University, *Dept. of Electronic Engineering, Southern Taiwan University of Technology

A novel 60-GHz wideband Marchand balun fabricated with a standard $0.18\mu\text{m}$ 6-metal-layer CMOS process is presented. A technique for achieving good balance with the fourth metal layer microstrip conductor is used in the designed Marchand balun. The fabricated CMOS balun uses multilayer coupling with the top two layers. An output matching network is added to improve the output return loss. The measured amplitude imbalance was about ± 1.5 dB from 25 to 65 GHz, over the 89% operating frequency band.

RTU1E-3 08:40 Room: HCC-315
De-Embedding Considerations for High Q RFIC Inductors

K. Goverdhanam, Y. Tretiakov, G. Ali Rezvani, S. Kapur*, D. E. Long*,
RF Micro Devices, *Integrand Software Inc.

In this paper, considerations for accurate de-embedding technique using the “open-thru” de-embedding methodology, aimed at de-embedding of high Q radio RFIC inductors will be presented. Also, proper design of on wafer GSGSG padset and de-embedding structures will be discussed. It will be shown, that accurate characterization of properly designed de-embedding structures results in very reliable and accurate de-embedding using the previously developed “open-thru” de-embedding method.

RTU1E-4 09:00 Room: HCC-315
A Low-Loss Compact Linear Varactor Based Phase-Shifter

J.H. Qureshi*, S. Kim**, K. Buisman*, C. Huang*, M. Pelk*,
A. Akhnoukh*, L.E. Larson**, L. K.Nanver*, L.C.N. deVreede*,
*Laboratory of High-Frequency Technology & Components TuDelft, Delft,
The Netherlands, **University of California at San Diego

Design trade-offs are presented for varactor-based variable phase-shifters in terms of size, tuning range, bandwidth/phase linearity and large-signal performance. Based on this study, a compact, low-loss ($0.6\text{dB}/90^\circ @ 1.0\text{ GHz}$), wideband and extremely linear varactor-based phase shifter is presented.

RTU1E-5 09:20 Room: HCC-315
Design and Layout Techniques for the Optimization of nMOS SPDT Series-Shunt Switches in a 130nm SiGe BiCMOS Technology

J. P. Comeau, J. D. Cressler, and M. Mitchell*, Georgia Institute of
Technology, *Georgia Tech Research Institute

This work investigates various design and layout optimization approaches for MOSFET-based series-shunt, SPDT switches in a commercially-available 130 nm SiGe BiCMOS technology. This experiment has yielded a SPDT switch with an insertion loss of -1.4 dB, 1.5 dB, and -2.0 dB, at 5.8 GHz, 10 GHz, and 20 GHz, respectively, and an input-referred third-order intercept point of 21 dBm at 9.5 GHz, without the use of any process adders or additional supply voltages.

Tuesday June 5, 2007

08:00

Room: HCC - 314

Session RTU1F: Novel Circuit Simulation and Modeling

Chair: Kevin McCarthy, University College Cork

Co-Chair: Bob Stengel, Motorola, Inc.

RTU1F-1

08:00

Room: HCC-314

Internal Unilateralization Technique for CMOS mm-Wave Amplifiers

B. Heydari, E. Adabi, M. Bohsali, B. Afshar, M.A. Arbabian, A.M. Niknejad, University of California at Berkeley

An internal unilateralization technique for cascode devices is analyzed and demonstrated in 90nm CMOS technology. The substrate network of the device has been incorporated in a circuit technique together with an LC tank on the top gate of the cascode structure. The structure is accurately modeled and conditions for unilateralization of the cascode are derived in terms of the LC tank parameters. An increase in the maximum stable gain from 7.5dB to 20dB has been verified in the measurements using this technique.

RTU1F-2

08:20

Room: HCC-314

Novel High-Q Inductor using Active Inductor Structure and Feedback Parallel Resonance Circuit

S. Seo, N. Ryu, H. Choi, Y. Jeong, *Dept. of Information & Communication Engineering, Chonbuk National University, Republic of Korea

This paper presents a novel high-Q inductor using grounded active inductor and feedback parallel resonance circuit. The novelty of the proposed structure is based on the increase of Q-factor by feeding parallel resonance circuit into grounded active inductor of gyrator structure. The high-Q inductor is fabricated by 0.18 μ m Hynix CMOS technology. The fabricated inductor shows inductance of above 45 nH and Q-factor of over 250 around 5GHz.

RTU1F-3 08:40 Room: HCC-314

Stability Analysis of On-Chip Multi-Stage RF Power Amplifier

M.Unterweissacher*, K. Mertens**, T. Brandtner**, W. Pribyl*,

*Department of Electronics TU-Graz, **Infineon Technologies Austria AG

On-chip multi-stage wideband power amplifiers may show oscillations due to an unwanted feedback loop via the power distribution network. A fully differential CMOS amplifier with a bandwidth from 6 to 9 GHz that was expected to be sensitive to oscillation has been analyzed by utilizing a novel pre-layout method for estimating power grid parasitics including inductance effects. Sweeping power grid model parameters enabled us to find a power grid that improved the stability of the power amplifier.

RTU1F-4 09:00 Room: HCC-314

Top-Down PLL Design Methodology Combining Block Diagram, Behavioral, and Transistor-Level Simulators

B. Nicolle* **, W. Tatinian*, J.-J. Mayol**, J. Oudinot**, G. Jacquemod*,

* LEAT, Sophia Antipolis, France, ** Mentor Graphics, St-Ismier, France

A design methodology based on a multi-simulator approach instead of co-simulation is presented. The study on a Phase Locked Loop (PLL) used in RF transceivers for frequency synthesis. We used Simulink as block diagram simulator, ADVance MS (ADMS) as behavioral simulator and Eldo as transistor-level simulator. The proposed results show the accuracy and simulation time for each description level.

RTU1F-5 09:20 Room: HCC-314

Nonlinear Behavioral Modeling of Passive RFID-Transponder-Frontends

K. Seemann, M. Hartmann, F. Cilek, A. Missoni*, G. Holweg**, R. Weigel,

University of Erlangen-Nuremberg, *University of Technology Graz,

**Infineon Technologies

A nonlinear RFID frontend behavioral model has been developed. By using this model the simulation time for inlay optimizations can be decreased considerably and the models hide the IC manufacturer's intellectual properties. The inherent model order reduction is based on nonlinear state-space mapping using derivative coordinates and harmonic-balance simulations. Feedforward multi-layer-perceptron artificial-neural-networks have been used for the nonlinear multivariate system mapping.

Tuesday June 5, 2007

13:20

Room: HCC - 313A

Session RTU3A: UWB and High-Frequency Front-Ends

Chair: Frank Henkel, IMST GmbH

Co-Chair: Georg Boeck, Berlin University of Technology

RTU3A-1

13:20

Room: HCC-313A

A 24-GHz CMOS Direct-Downconversion Sub-Harmonic Downconverter

R. M. Kodkani, L. E. Larson, Center for Wireless Communications, Dept of Electrical & Computer Engineering, University of California, San Diego

A 24 GHz sub-harmonic mixer based downconverter is presented. Fabricated in a 0.13 μm CMOS process the downconverter includes a pre-amplifier and an IF buffer and consumes 14.4 mW with a 1.6 V supply. The quadrature LO buffer consumes 15 mA at 1.2 V. The circuit includes a single-ended to differential phase splitter for the LO. The downconverter has a conversion gain of 3.2 dB and DSB Noise Figure of 10 dB. The measured input referred 1 dB compression point is -12.7 dBm.

RTU3A-2

13:40

Room: HCC-313A

A 1.2-V, 5.8-mW, Ultra-Wideband Folded Mixer in 0.13- μm CMOS

K. H. Choi, D. H. Shin*, C. P. Yue*, Dept. of ECE, Carnegie Mellon University, Dept. of ECE, University of California, Santa Barbara*

This paper presents the design and analysis of a low-voltage down-conversion mixer in 0.13- μm CMOS for ultra-wideband (UWB) applications between 3–7 GHz. The effects of supply voltage, current density, and LO amplitude on the mixer performance are studied. The DC offset of the mixer is measured systematically to isolate the contributions due to the different sources including device mismatch, self-mixing, and second-order intermodulation.

RTU3A-3 14:00 Room: HCC-313A

A Broadband CMOS Multiplier-Based Correlator for IR-UWB Transceiver SoC

H. Xie, X. Wang, A. Wang, Dept. of Electrical & Computer Engineering, Illinois Institute of Technology

An multiplier-based correlator is an important component for impulse radio ultra-wideband receiver. This paper reports design of a fully integrated low-power multiplier-based correlator for a 3.1-10.6GHz UWB receiver in 0.18 μ m CMOS that consists of a UW multiplier and a RC integrator with a 200MHz bandwidth. Measurement results confirm the correlation-type demodulation function and achieve a conversion gain of 0dB, noise figure of 8.2dB and a power consumption 52mW for the UWB multiplier.

RTU3A-4 14:20 Room: HCC-313A

A 3 to 9-GHz Dual-band Up-Converter for a DS-UWB Transmitter in 0.18-micron CMOS

M. Annamalai, Y. Zheng, W.G. Yeoh, Institute of Microelectronics, Singapore.

A dual-band up-converter(DB-UPC) for a direct sequence UWB transmitter is demonstrated on 0.18 μ m CMOS. The DB-UPC translates a UWB pulse to a 3-5GHz low-band or 7-9GHz high-band. The DB-UPC consists of high and low-band mixers followed by combiner. The mixers consist of a differential core followed by a differential to single-ended converter. The DB-UPC is linear for up to 0.7Vpp input pulse. Measured voltage gain and IIP3 are -8dB, +10dBm for low-band and -14dB, +14dBm for high-band.

RTU3A-5 14:40 Room: HCC-313A

A Miniature, Folded-Switching, Up-conversion Mixer for UWB Applications Using 0.18- μ m CMOS Process

P.-C. Huang, F.-C. Chang, S.-F. Chao, H. Wang, National Taiwan University, Taipei, Taiwan

This paper presents a compact up-conversion mixer using commercial 0.18- μ m CMOS technology for UWB system applications. To achieve broadband frequency response, low power consumption, and small chip size simultaneously, the folded structure and inductor-ree matching network are adopted. The measured mixer demonstrates a measured wideband response from 1 to 11 GHz with a conversion loss of lower than 6 dB. The dc power consumption is 25 mW under a supply voltage.

Tuesday June 5, 2007

13:20

Room: HCC - 313B

Session RTU3B: Wideband Potpourri

Chair: Jacques C Rudell, Intel Corporation

Co-Chair: Stefan Heinen, Infineon Technologies AG

RTU3B-1

13:20

Room: HCC-313B

INVITED: Power-Efficient Decision-Feedback Equalizers for Multi-Gb/s CMOS Serial Links

J. F. Bulzacchelli, A. V. Rlyakov, D. J. Friedman, IBM Research Division

This paper presents three different DFE circuits with power dissipations between 4.8 and 9.3 mW and data rates in the range of 6-10 Gb/s. One DFE uses a soft decision technique to reduce the critical path delay of the first feedback tap. The other two employ speculation to relax the critical timing. Speculation increases the number of parallel data paths, but the power dissipation of each path is kept low with power-efficient summer designs based on switched-capacitors or current integration.

RTU3B-2

13:40

Room: HCC-313B

A Single-chip DBS Tuner-Demodulator SoC Using Discrete AGC, Continuous I/Q Correction and 200MS/s Pipeline ADCs

A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, T. Nutt, D. Trager, Silicon Laboratories Inc., Austin, TX

A digital low-IF satellite TV tuner-demodulator SoC was realized in 0.13 μ m CMOS using low power 200MS/s eight bit pipeline ADCs. A discrete-steps delayed AGC loop using FET switched-resistors resulted in a 10dB noise figure at max gain and +25dBm IIP3 at min gain. The image rejection correction is continuously performed in the digital domain using an inverse gain and phase mismatch adjustment. An FFT engine was used for carrier/symbol rate estimation and channel blind scanning.

RTU3B-3 14:00 Room: HCC-313B
Heterogeneously Integrated 10Gb/s CMOS
Optoelectronic Receiver for Long Haul
Telecommunication

H. Sharifi, S. Mohammadi, Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University

A fully integrated 10Gb/s 1.3 to 1.55 μ m optoelectronic receiver is demonstrated for the first time. By heterogeneously integrating of a CMOS transimpedance amplifier (TIA) with an InGaAs/InP PIN photodiode using a recently developed self-aligned wafer-level integration technology (SAWLIT) operation at 10Gb/s is achieved. The CMOS transimpedance amplifier exhibits a transimpedance gain of 51dB and a bandwidth of 6.1GHz.

RTU3B-4 14:20 Room: HCC-313B
Tuned LC Clock Buffers with Static Phase Adjust

V. P. Reddy, W. S. Titus, J. G. Kenney, Analog Devices Inc.

An LC tank providing clock buffering for a half-rate binary phase detector in a clock and data recovery circuit is described. This paper analyzes the trade-offs involved in choosing the Q of the LC tank, presents an automatic tuning method for the LC tank and describes a method to program the phase of the clock relative to the input data using 2 LC tanks with mismatched center frequencies. This work is part of a transceiver chip for XFP fiber optic application fabricated in a 0.13 μ m CMOS process.

Tuesday June 5, 2007

13:20

Room: HCC - 301A

**Session RTU3C: Microwave and mm-Wave
Synthesizers and Components**

Chair: Sanjay Raman, Virginia Tech

Co-Chair: Lawrence Kushner, Kenet, Inc

RTU3C-1 13:20 Room: HCC-301A

**Performance and Yield Optimization of mm-Wave
PLL Front-End in 65nm SOI CMOS**

D. Lim, J. Kim*, J.-O. Plouchart*, D. Kim*, C. Cho*, D. S. Boning,
Massachusetts Institute of Technology, *IBM, Hopewell Junction, NY

A combination of 70GHz LC-VCO and 2:1 CML static frequency divider has been fabricated in 65nm SOI CMOS technology. A cas-coded buffer amplifier is used in VCO-to-divider connection and inductive peaking is employed for bandwidth enhancement. The bias condition of the frequency divider has been tuned to find an optimal bias point in the existence of VCO and divider operating range variation. The inter-die VCO and divider variations over a wafer and their correlation have been estimated.

RTU3C-2 13:40 Room: HCC-301A

**A 16 to 19-GHz Sub-Integer Frequency Synthesizer for
a 60-GHz Transceiver**

B. A. Floyd, IBM T. J. Watson Research Center

A 16.3 to 19-GHz frequency synthesizer is implemented in 0.13- μ m SiGe BiCMOS technology as part of a 60-GHz transceiver chipset. It provides for RF channels of 56.5-64 GHz in 500-MHz steps, and features a phase-rotating multi-modulus sub-integer divider. The measured RMS phase noise of the synthesizer is 1.7 deg, while phase noise at 100-kHz and 10-MHz offsets are -93 and -115 dBc/Hz, respectively. Reference and sub-integer spurs are between -48 to -70 dBc, and power consumption is 118 mW.

RTU3C-3 14:00 Room: HCC-301A

A 16mW 8Mbps Fractional-N FSK Modulator at 15.8-18.9GHz

M. Straayer, A. Messier, and T. Hancock, MIT Lincoln Laboratory, Lexington, MA

Indirect modulation of fractional-N synthesizers is an energy-efficient architecture capable of moderate data rates, and is well-suited for use in sensor networks or WLAN. This work implements a fully-integrated fractional-N synthesizer optimized for power efficient modulation at 15.8 to 18.9GHz with an 80MHz reference. Binary and 4-ary FSK modulation of up to 8Mbps is achieved while consuming 16mW in IBM 0.18 μ m SiGe BiCMOS.

RTU3C-4 14:20 Room: HCC-301A

A 15-GHz 7-channel SiGe:C PLL for 60-GHz WPAN Application

J.-Y. Lee, S.-H. Lee, H. Kim, H.-K. Yu, Electronics and Telecommunications Research Institute

In this paper, we present the design of 15-GHz frequency synthesizer for 60-GHz WPAN. The PLL generates 7 channels of output signals with 250 MHz step by using the high-speed programmable divider operating up to 10 GHz. A double cross-coupled LC VCO is used for achieving higher oscillation frequency and shows about 20% tuning range. The PLL represents phase noise of -85 dBc/Hz at 100 kHz offset from 15.75 GHz and consumes 115 mA at 2.5 V supply voltage.

RTU3C-5 14:40 Room: HCC-301A

A Ka Band, Static, MCML Frequency Divider, in Standard 90nm-CMOS LP for 60 GHz Applications

H.M.Cheema, R.Mahmoudi, A.H.M.van Roermund, M.A.T. Sanduleanu*, Department of Electrical Engineering, Eindhoven University of Technology, The Netherlands, *Philips Research, Eindhoven, The Netherlands.

This paper presents a broadband, static, 2:1 frequency divider in a bulk 90nm CMOS LP technology with maximum operating frequency of 35.5 GHz. The divider exhibits an enhanced input sensitivity, below 0 dBm, over a broad input range of 27 GHz and consume 24mA from a 1.2 V supply. The phase noise of the divider is -107.7 dBc/Hz at 1MHz offset from the carrier.

Tuesday June 5, 2007

13:20

Room: HCC - 301B

Session RTU3D: Silicon technology for mm-Wave ICs

Chair: Marko Sokolich, HRL Laboratories

Co-Chair: Mahesh Kumar, Lockheed Martin

RTU3D-1 13:20 Room: HCC-301B

**INVITED: Silicon Schottky Diode Power Converters
Beyond 100 GHz**

C. Mishra*, U. Pfeiffer**, R. Rassel***, S. Reynolds****, * Was with IBM Research, now with Texas A & M Univ. ** Was with IBM Research, now with Univ. of Siegen, Germany. ***IBM Systems & Technology Group **** IBM Research

This paper presents circuits based on Schottky barrier diodes (SBDs) in IBM's 0.13- μm SiGe BiCMOS process. Circuits such as sub-harmonic up-conversion mixers and frequency doublers are demonstrated at frequencies beyond 100 GHz on silicon. These circuits enable power generation at millimeter wave frequencies on silicon. The frequency doublers can deliver >0 dBm output power at 110 GHz and the 2X sub-harmonic up converters exhibit peak conversion loss of <3 dB up to 120 GHz.

RTU3D-2 13:40 Room: HCC-301B

**Hot Carrier Degradation and Performance of 65nm
RF n-MOSFET**

M. Fakhruddin,* M. C. Tang,** J. Kuo,* J. Karp,* D. Chen,** C S Yeh,** and S C Chien,**, *Xilinx, Inc., **United Microelectronics Corp.

Hot carrier stress (HCS) induces significant degradation on the performance of 65nm RF n-MOSFET with minimum poly length (L_{poly}). Although the cutoff frequency (f_t) is record high 212 GHz for these devices, the high HCS degradation poses a challenge for RF application. Additional effort will be needed to improve the process and/or device to take full advantage of the record n-MOSFET performance.

RTU3D-3 14:00 Room: HCC-301B

65 nm HR SOI CMOS Technology: Emergence of Millimeter-Wave SoC

F. Giancesello*, S. Montusclat*, B. Martineau**,*, D. Gloria*, C. Raynaud*,***, S. Boret*, G. Dambrine**, S. Lepilliet** and R. Pilard*, *STMicroelectronics, FTM, TPS Lab, Crolles (FRANCE), **IEMN Villeneuve d'Ascq (FRANCE), ***CEA Leti Grenoble (FRANCE)

Today, measurement of 65 nm CMOS and 130nm-based SiGe HBTs technologies demonstrate both f_t and f_{max} higher than 200 GHz. The integration of transceiver at 60 GHz has been achieved. Passive circuits working @ 220 GHz have been achieved on High Resistivity SOI. HR SOI has also demonstrated some advantages concerning the performances of integrated antennas. This paper will review the MMW performances of stmicroelectronics 65 nm CMOSHR SOI technology and discuss the opportunities of MMW soc.

RTU3D-4 14:20 Room: HCC-301B

Novel Collector Structure Enabling Low-Cost Millimeter-Wave SiGe:C BiCMOS Technology

J.P. John, J. Kirchgessner, D. Morgan, J. Hildreth, M. Dawdy, R. Reuter, and H. Li, Freescale Semiconductor

A millimeter-wave selective-epi, SiGe:C HBT is described, utilizing a novel, low-cost collector construction. A cutoff frequency (f_T) of 200GHz and a maximum oscillation frequency (f_{MAX}) of 300GHz is achieved using a self-aligned selective-epi base structure. For a SiGe: C HBT, this is the highest known f_{MAX} obtained without the use of buried layer or deep trench isolation.

RTU3D-5 14:40 Room: HCC-301B

Vertical-Ground-Plane Transmission Lines for Miniaturized Silicon-Based MMIC

J.-W. Huang, C.-S. Wang, C.-K. Wang, S.-H. Yeh*, Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, *Industrial Technology Research Institute, Hsin-Chu, Taiwan

This paper presents a compact transmission line (TL) structure, which comprises one signal line surrounded by two vertical ground planes (VGPs). A V-band amplifier using VGP TLs for matching is also implemented in a 0.13- μ m CMOS technology with a peak gain of 18.3 dB at 52 GHz with a compact area of only 0.36mm² while consuming 16mW from a 1.2-V supply. Compared to other V-band CMOS amplifiers using TLs for matching, this amplifier has the lowest power consumption and the smallest chip size.

Tuesday June 5, 2007

15:30

Room: HCC - 313A

Session RTU4A: Advanced Transmitter Building Blocks

Chair: Freek van Straten, NXP Semiconductor

Co-Chair: David Ngo, RFMD

RTU4A-1

15:30

Room: HCC-313A

Ka-Band Low-Loss and High-Isolation 0.13 Micron CMOS SPST/SPDT Switches Using High Substrate Resistance

B. Min, G. M. Rebeiz*, University of Michigan at Ann Arbor, *University of California at San Diego

This paper presents 35 GHz SPST/SPDT CMOS switches using a 0.13 μm BiCMOS process. The MOSFETs are designed to have a high substrate resistance to minimize the insertion loss and improve power handling capability. The SPST/SPDT switches have a insertion loss of 1.9 dB/2.3 dB, and an input P1dB of >22 dBm. The isolation is >30 dB at 35-40 GHz and is achieved using two parallel resonant networks. To our knowledge, this is the first demonstration of low-loss, high-isolation switches at Ka-band.

RTU4A-2

15:50

Room: HCC-313A

RF-MEMS Based Adaptive Antenna Matching Module

A. V. Bezooijen, F. v. Straten, J. Snee*, R. Mahmoudi**, A.H.M. v. Roermund**, NXP Semiconductors, Nijmegen, The Netherlands.

*NXP Semiconductors, Eindhoven, The Netherlands. **Eindhoven University of Technology, The Netherlands.

To preserve link quality, in fluctuating operating environments, an adaptive antenna matching module is presented that consists of an 5-bit RF-MEMS switched capacitor array, a bipolar 60/30V MEMS-biasing voltage generator for improved reliability, and an phase detector that provides information on mismatch. It uses an iterative up-down counting algorithm for robust control. Measurements show proper correction of the antenna reactance, even for a VSWR of 10.

RTU4A-3

16:10

Room: HCC-313A

An 8-GHz Beamforming Transmitter IC in 130-nm CMOS

J. Wernehag, H. Sjöland, Department of Electroscience, Lund University

An 8-GHz beamforming transmitter IC has been designed in a 130-nm CMOS process. Two power amplifiers with independently controllable phase enable the beamforming. The phases are digitally controllable over full 360 degree range, which is accomplished binary weighting of quadrature phase signals in the power amplifiers. The quadrature phase signals are generated by a quadrature voltage controlled oscillator followed by a buffer, which serves as an isolation between the power amplifier.

RTU4A-4 16:30 Room: HCC-313A
A Spectrally Pure 5.0 W, High PAE, (6-12 GHz)
GaN Monolithic Class E Power Amplifier for Advanced
T/R Modules

R. Tayrani, Raytheon Space & Airborne Systems

This paper introduces a new highly efficient broadband monolithic class-E power amplifier utilizing a single 0.25 μm x 800 μm AlGaIn/GaN field-plated HEMT producing 8 W/mm of power at 10.0 GHz. The HPA utilizes a novel distributed broadband class-E load topology to maintain a simultaneous high PAE and output Power over (6-12 GHz). The HPA's peak PAE and output power performance measured under three pulsed drain voltages at 7.5 GHz are: (67%, 36.8 dBm @ 20 V), (64%, 37.8 dBm @ 25 V) and (58%, 3.3 dBm @ 30 V). The new broadband load also provides a spectrally pure output power response under CW and pulsed modulated RF input conditions. The HPA spurious free performance is evident from its low AM and PM noise figures of <-125 dBc at 10 KHz from carrier and <-130 dBc at 15 KHz from 10 GHz respectively. To the best of our knowledge, this is the highest ever reported performance for a high power, 6-12 GHz GaN class-E power amplifier.

RTU4A-5 16:50 Room: HCC-313A
1-Watt Conventional and Cascoded GaN-SiC Darlington
MMIC Amplifiers to 18 GHz

K. W. Kobayashi, *Y. C. Chen, *I. Smorchkova, *R. Tsai, *M. Wojtowicz, *A. Oki, Sirenza Microdevices, *Northrop Grumman Space & Technology

A 0.2 μm T-gate GaN-SiC HEMT technology with $f_T \sim 70$ GHz are used to achieve GaN Darlington MMIC Amplifiers with bandwidths up to 18 GHz. Both conventional Darlington and Cascoded-Darlington feedback designs were fabricated and measured. The Darlington ascode obtains 14.7 dB gain and a bandwidth of 0.05-12.3 GHz. The conventional Darlington obtains 11 dB gain and a record 0.05-18.7 GHz multi-decade bandwidth for a GaN Darlington. These are the highest BWs reported for GaN Darlington MMIC amp.

Tuesday June 5, 2007

15:30

Room: HCC - 313B

Session RTU4B: New Trends in VCO Techniques

Chair: Jinghong Chen, Analog Devices

Co-Chair: Tian-Wei Huang, National Taiwan University

RTU4B-1 15:30 Room: HCC-313B

A Compact 5GHz Standing-Wave Resonator-based VCO in 0.13 μ m CMOS

D. Shi, J. East and M. P. Flynn, University of Michigan

A novel on-chip capacitively-loaded, transmission-line-standing-wave resonator is employed in a low phase noise VCO, to achieve a measured phase noise of -117dBc/Hz at a 1MHz offset. The prototype 5GHz VCO, implemented in 0.13 μ m CMOS, dissipates 3mW from a 1.2V supply, and occupies a compact die area of 0.11mm².

RTU4B-2 15:50 Room: HCC-313B

A Dual Band, Wide Tuning Range CMOS Voltage Controlled Oscillator for Multi-Band Radio

Burak Catli, Mona M. Hella, Rensselaer Polytechnic Institute

A novel multi-band VCO is presented, using a double-tuned, current-driven transformer load. The dual frequency range oscillator (low band and high band), is based on the ON/OFF switching of current in the secondary port of the transformer. The concept is validated through measurement results from a fabricated prototype in 0.25 μ m CMOS technology. The VCO has a measured tuning range of 1.94 to 2.55GHz for the low-frequency band and 3.6 to 4.77GHz for the high-frequency band. It draws a current of 1.0 mA from 1.8V supply with a phase noise of -116dBc/Hz at 1MHz offset from 2.55GHz carrier. For the high frequency band, it draws 7.5mA from the same supply with a phase noise of -106dBc/Hz at 1MHz offset from 4.77GHz carrier.

RTU4B-3 16:10 Room: HCC-313B
Double Cross Coupled Colpitts VCO with Low Phase Noise using InGaP/GaAs HBT Technology

B. Shrestha, N. Y. Kim, RFIC Research and Education Center, Kwangwoon University

The proposed double cross-coupled differential Colpitts voltage controlled oscillator (VCO) is designed, using InGaP/GaAs HBT technology for an adaptive feedback interference cancellation system (AF-ICS). The VCO achieves excellent phase noise characteristics of -135 dBc/Hz at 1 MHz offset from carrier frequency (1.630 GHz) when supplied with a control voltage of 0 V. Its tuning range is around 218 MHz with an output power of -3.91 dBm. It shows the figure of merit (FoM) of -180 dBc/Hz.

RTU4B-4 16:30 Room: HCC-313B
A 12-GHz Low Phase Noise VCO By Employing Novel CMOS Field-Plate Transistors

C.-C. Wei, H.-C. Chiu, W.-S. Feng, Chang Gung University, Taiwan

This paper presents a voltage-controlled oscillator (VCO) with low phase noise by employing the CMOS field-plate (FP) transistors. The proposed FP transistors perform the improvement in flicker noise ($1/f$ noise) was demonstrated in our previous investigation. A complete large-signal model for FP transistors was established by modified BSIM4 model with lossy substrate network. The proposed low phase noise 12-GHz VCO with FP transistors was designed and fabricated in TSMC 0.13- μ m CMOS process.

RTU4B-5 16:50 Room: HCC-313B
A tuned-input tuned-output VCO in 0.18micron CMOS

S. Shekhar, S. Aniruddhan*, D.J. Allstot, University of Washington, Seattle, *Qualcomm Inc., San Diego

A fully-integrated 2.3-2.7GHz differential voltage-controlled oscillator derived from the classical tuned-input tuned-output (TITO) topology in 0.18 μ m CMOS is presented. It uses an auxiliary resonant tank for additional noise suppression and achieves measured phase noise values of -110 dBc/Hz and -130.5 dBc/Hz at 100 kHz and 1 MHz frequency offsets, respectively. With a current consumption of 7.5mA from a 1.8V supply, it attains a figure-of-merit of 187.2dBc/Hz.

Tuesday June 5, 2007

15:30

Room: HCC - 301A

Session RTU4C: Advances in Low-Noise Amplifiers

Chair: Brian A. Floyd, IBM

Co-Chair: Leonard D. Reynolds, RFMD

RTU4C-1

15:30

Room: HCC-301A

A gm-Boosted Current-Reuse LNA in 0.18micron CMOS

J. S. Walling, Sudip Shekhar, D. J. Allstot, University of Washington

In this paper a design which enhances the performance of the CG LNA is detailed. The noise performance is improved through the use of a gm-boosting technique, while the gain performance is improved using current-reuse techniques. The proposed solution alleviates the issues related to the more frequent CS-CS current-reuse topologies. The technique is validated with a design in 0.18um CMOS, with a 5.4GHz LNA which achieves >20dB of gain, <3dB NF and consumes only 2.7mW of power.

RTU4C-2

15:50

Room: HCC-301A

A 2.4-GHz 0.82-mW Hybrid Balun for Low-Power Fully-Differential Direct Conversion Receivers in 0.18micron CMOS

H. Shin, J. Park, Kwangwoon University

A low-power, low-noise, and highly-linear hybrid balun circuit is proposed for fully-differential low-power CMOS RF receivers. The hybrid balun is composed of a passive transformer and loss-compensating amplifiers. Design considerations are discussed regarding the optimal signal coupling and phase matching. A 2.4-GHz hybrid balun in 0.18-um CMOS achieves 2.8-dB higher gain and 1.9-dB lower noise figure than its passive counterpart and +23dBm of IIP3 only at a power consumption of 0.82-mW.

RTU4C-3 16:10 Room: HCC-301A
A Wide-Band CMOS Variable-Gain Low Noise Amplifier for Multi-Standard Terrestrial and Cable TV Tuner

D.G. Im, *S.S. Song, H.T. Kim, and *K. Lee, LG Electronics Institute of Technology, *Korea Advanced Institute of Science and Technology

A CMOS wide-band low noise amplifier (LNA) based on the current amplification for the multi-standard terrestrial and cable tuner is proposed. By adopting the structure combined the common source amplifier with the common gate amplifier by the current amplification, the noise figure does not have any influence on wide-band input matching so that we can achieve low noise figure by the noise canceling and excellent wide-band input matching at the same time while allowing some variable gains.

RTU4C-4 16:30 Room: HCC-301A
30 GHz CMOS Low Noise Amplifier

E. Adabi, B. Heydari, M. Bohsali and A. M. Niknejad, University of California at Berkeley

A 30GHz low noise amplifier was designed and fabricated in a 90nm digital CMOS process. The mm-wave amplifier has a peak gain of 20dB at 28.5GHz and a 3dB bandwidth of 2.6GHz with the input and output matching better than 12 and 17dB over the entire band respectively. The NF is 2.9dB at 28GHz and less than 4.2dB across the band. It can deliver 2dBm of power to a matched load at its 1dB compression point and the measured IIP₃ is -7.5dBm. The amplifier consumes 16.25mW of power out of 1V supply.

RTU4C-5 16:50 Room: HCC-301A
A 2 mW, Sub-2 dB Noise Figure, SiGe Low-Noise Amplifier For X-band High-Altitude or Space-based Radar Applications

T. K. Thrivikraman, W.-M. L. Kuo, J. P. Comeau, A. K. Sutton, J. D. Cressler, P. W. Marshall*, M. A. Mitchell**, Georgia Institute of Technology, *Consultant to NASA, ** Georgia Tech Research Institute

This paper presents a low-power X-band low-noise amplifier (LNA) implemented in silicon-germanium (SiGe) technology targeting high-altitude or space-based low-power density phased-array radar systems. To our knowledge, this X-band LNA is the first in a Si-based technology to achieve less than 2 dB mean noise figure while dissipating only 2 mW from a 1.5 V power supply. The gain of the circuit is 10 dB at 10 GHz with an IIP₃ of 0 dBm.

Tuesday June 5, 2007

15:30

Room: HCC - 301B

Session RTU4D: MOSFET Characterization and Modeling

Chair: Yuhua Cheng, Siliconlinx, Inc.

Co-Chair: Bumman Kim, Pohang University of Science
and Technology

RTU4D-1

15:30

Room: HCC-301B

**A New Approach of High Frequency Noise Modeling for
70-nm NMOS by Accurate Noise Source Extraction**

Y. Kiyota, C - H. Chen *, T. Kubodera, A. Nakamura, K. Takeshita, and
M. J. Deen *, Semiconductor Business Group, Sony Corporation,*
Electrical and Computer Engineering Department, McMaster University

Noise sources of 70-nm NMOS transistors were extracted to reveal the channel noise is dominant up to 26 GHz. A new approach to accurately capturing the behavior of thermal noise by compensating for the discrepancy between extracted and simulated channel noise through the addition of an excess noise source was demonstrated. By using this technique the noise figure of MOS transistors at any source impedance values can be simulated correctly.

RTU4D-2

15:50

Room: HCC-301B

**A New Noise Parameter Model of Short-Channel
MOSFETs**

J. Jeon, I. M. Kang, Y. Yun, B.-G. Park, J. D. Lee, H. Shin, School of
Electrical Engineering, Seoul National University

In this paper, a closed form expression for noise parameters of MOSFETs are derived from a more accurate small-signal equivalent circuit. The modeling results show a good agreement with the measured data. Based on the analysis of the noise coming from channel thermal noise and parasitic resistances, the noise contribution from each component is analyzed.

RTU4D-3 16:10 Room: HCC-301B
CR018 Wideband Noise Model for AMS/RF CMOS Simulation

M.T. Yang, C.W. Kuo, P.P.C. Ho, D.C.W. Kuo, C.C. Chen, T.J. Yeh, Charles Tseng*, J. Jayapalan*, G. Brown*, G. Yeap*, Y. Du*, S. Liu, TSMC, Inc., *Qualcomm, Inc.

The experimental verification of CR018 wideband noise model for AMS/RF CMOS simulation was realized. Among which, independent Flicker noise corner model scaling with device size was developed. In addition, the corner frequency was measured and validated experimentally. A good fit of thermal noise using SPICE2 model with $\gamma=2/3$ was achieved. Moreover, the effects of induced gate and bulk noises will be investigated. Finally, sanity checks of noise model will be addressed with switch cap and VCO.

RTU4D-4 16:30 Room: HCC-301B
MOSFET Model Extraction Using 50GHz Four-Port Measurements

J. Brinkhoff, S. C. Rustagi, J. Shi, F. Lin, Institute of Microelectronics, Singapore

An accurate and efficient method to extract an equivalent circuit model of a MOSFET is presented. Four-port measurements simplify the determination of important elements, such as the substrate networks. These measurements are also used to extract the MOSFET extrinsic parasitic elements. The accuracy of the model extraction is verified by simulation and measurement to 50 GHz.

RTU4D-5 16:50 Room: HCC-301B
Distortion simulations with the PSP Model: Common-gate circuits

C. M. Olsen, L. F. Wagner, J. Watts, J. R. Jones, J. J. Pekarik, IBM Semiconductor Research and Development Center

We present extensive simulations of distortion in common-gate configured FETs, operated around $V_{ds}=0V$, using the new PSP MOSFET model. We compare results to measurements. As the FET is configured into an increasingly more realistic circuit, the PSP models distortion performance improves correspondingly and it can predict intermodulation distortion within $\sim 3dB$ of measured data. We quantify IMD improvement as function of the gate length and show that longer FETs have lower distortion.

Tuesday June 5, 2007

14:00 - 17:00

Room: HCC - Ballroom A

Session RTUP: Interactive Forum

Chair: Tina Quach, Freescale Semiconductor

Co-Chair: Jenshan Lin, University of Florida

RTUP-01

Coherent BPSK Demodulator MMIC Using an Anti-Parallel Synchronization Loop,

Y. Zheng, C. E. Saavedra, Queen's University, Kingston, ON, Canada

A coherent BPSK demodulator using an anti-parallel synchronization loop is successfully implemented in a 0.18 μm CMOS monolithic-microwave-integrated-circuit (MMIC). Due to the novel concept of the anti-parallel synchronization method, the demodulator only requires a differential VCO as opposed to a quadrature VCO as in the Costas Loop, thereby saving considerable chip space. The fabricated demodulator works at a carrier frequency of 2.7 GHz and has been tested at data rates of up to 7 Mbps.

RTUP-02

A 0.13 μm CMOS 5GHz Fully Integrated 2x3 MIMO Transceiver IC with over 40dB Isolation

R. Tachibana, S. Kousai*, T. Kato, H. Kobayashi*, R. Ito, A. Maki*, D. Miyashita*, Y. Araki, T. Hashimoto, H. Hoshino, T. Sekiguchi, M. Ashida*, I. Seto, M. Hamada*, R. Fujimoto*, H. Yoshida, S. Otaka, Toshiba Corp., *Toshiba Corp. Semiconductor Company

A 5GHz MIMO direct conversion transceiver composed of 2 transmitters (TXs) and 3 Receivers (RXs) is fabricated with 0.13 μm CMOS technology. Die size is 4.56mm x 7.7mm. For driving 10GHz LO signal lines of 5mm length, inductor-less low-power LO repeaters are equipped in individual LO paths. Isolation of over 40dB is obtained by equipping separate GNDs on both the MIMO IC and the circuit board. TX EVM of over -31dB is obtained at -8.6dBm for 2 TX mode when external LO of 10GHz is applied.

RTUP-03

A 5 x 5 mm Highly Integrated Dual-band WLAN Front-End Module Simplifies 802.11 a/b/g and 802.11n Radio Designs

C.-W. P. Huang, W. Vaillancourt, C. Masse, J. Soricelli, T. Quaglietta, A. Long, G. Rabjohn, A. Parolin, SiGe Semiconductor, Ottawa, Canada

A highly integrated 5 x 5 x 0.9 mm dual-band WLAN front-end module that significantly simplifies 802.11 a/b/g and 802.11n radio designs is presented. The FEM features 29 dB gain and 18.5 dBm at 54 Mbps with EVM < 3% and 160 mA for 2.4 to 2.5 GHz. For 4.9 to 5.9 GHz, the FEM delivers 25 dB gain and 16.5 dBm with EVM < 3% and 195 mA. The receive chains can be realized either with LNA having >11 dB gain with NF < 2.5 dB for the low band and < 2.8 dB for the high band or with a < 1 dB loss diplexer.

RTUP-04

A 5.2 GHz BFSK Receiver with On-Chip Antenna for Self-Powered RFID Tags and Medical

P. H. R. Popplewell, V. Karam, A. Shamim, J. Rogers, C. Plett, Carleton University

A completely integrated FM receiver design for short range wireless applications is presented. The complete SoC solution uses an on-chip antenna and consumes an average of 850 μ W in transmit mode (at a 5 kb/s data rate) and 5.5 mW while receiving. A thin film ultra capacitor and solar cell can be stacked on top of the chip to power the radio; yielding a completely integrated solution. The current injection-locked design has a communication range of 1.75 m which can be increased with tradeoffs.

RTUP-05

Achieving Wideband sub-1dB Noise Figure and High Gain with MOSFETs if Input Power Matching is not Required

E.A.M. Klumperink, Q. Zhang, G. J. M. Wienk, R. Witvers*, J. G. Bij de Vaate*, E.E.M. Woestenburg*, B. Nauta, University of Twente, CTIT, IC-Design at Enschede, The Netherlands, * ASTRON at Dwingeloo, The Netherlands

A 0.18 μ m CMOS Low Noise Amplifier (LNA) achieves sub-1dB Noise Figure (NF) over more than an octave of bandwidth without external noise matching components. It is designed for a future radio telescope, requiring millions of cheap LNAs mounted directly on antenna elements. At 90mW power, sub-1dB NF is achieved for 50 source impedance over a 0.8-1.8GHz band without external coils, and $S_{21} > 20$ dB, $OIP_2 > 25$ dBm and $OIP_3 > 15$ dBm. Preliminary results for 150 source impedance show NF=0.35dB around 900MHz.

RTUP-06

A Bondpad-Size Narrowband LNA for Digital CMOS

J. Borremans* **, P. Wambacq* **, G. Van der Plas**, Y. Rolain*, M. Kuijk*, *Vrije Universiteit Brussel, Brussels, Belgium, **IMEC, Leuven, Belgium

The need for a high level of integration in wireless and multi-standard radios, as well as the expensive area in downscaled CMOS pushes towards low-area circuit solutions. Feedback-type inductorless LNAs are such an example. This paper demonstrates a bond pad-size feedback type narrowband LNA using only one stacked inductor. The gain is 20.8 dB at 3.4 GHz with a NF of 2.2 dB. This solution is many times smaller than a classical LNA configuration with several inductors, for similar performance.

RTUP-07

Fully Integrated High-Q Switched Capacitor BandPass Filter with Center Frequency and Bandwidth Tuning

A. El oualkadi, M. El Kaamouchi*, D. Flandre, Université Catholique de Louvain, Belgium

This paper proposes to study the design of a novel high-Q fully integrated switched capacitor bandpass filter. This circuit, implemented in CMOS technology, allows a tunable high selectivity over a broad frequency band. The proposed architecture is intoned to replace passive surface acoustic wave (SAW) filters in radio-communication applications. A prototype has been fabricated. Measurements show quality factors up to 300, and a tunable center frequency range of 290 MHz with a bandwidth tuning.

RTUP-08

60-GHz LNA Using a Hybrid Transmission Line and Conductive Path to Ground Technique in Silicon

J. Alvarado Jr., K. T. Kornegay, D. Dawn*, S. Pinel*, J. Lasker*, Cornell University and Georgia Institute of Technology, *Georgia Institute of Technology

A monolithic 60GHz low-noise amplifier (LNA) using a passive noise suppression technique and an enhanced hybrid transmission line structure, fabricated in a 0.12 μ m SiGe BiCMOS process is presented. Measurements of the single-stage LNA at 59GHz show a gain of 13.8dB, a NF of 4.1dB, using 4.5mA from a 1.8v supply. Across the entire V-band (57 - 64GHz), the LNA has a minimum gain of 12dB and average NF of 5dB. This LNA has the highest known figure of merit reported for a 60GHz application.

RTUP-09

A Low Distortion FM Tuner Analog Front-End with Multi-tanh Low Noise Amplifier

J. Hu, M. R. May*, M. D. Felder*, L. DiSanza*, L. H. Ragan, The University of Texas at Austin, *SigmaTel, Inc.

An analog front-end (AFE) of a frequency modulation (FM) tuner is presented in this contribution. The proposed AFE consists of a tunable antenna interface and a variable-gain two-stage low-noise amplifiers (LNA). The AFE can be tuned to resonate at FM frequencies ranging from 63 MHz to 129 MHz. The LNA achieves a voltage gain adjustable from -1.5 dB to 30.5 dB across the FM band. By employing the multi-tanh design principle in the LNAs, the linearity of the AFE is improved by 5 dB and 9 dB in the low and high gain modes of the LNA, respectively. The whole AFE is fabricated in a TSMC 0.18 μ m CMOS technology. It draws maximum 5.5 mA current from a 1.35-V supply and occupies 0.15 mm² of chip area. Both experimental and simulation results are provided to demonstrate the performance of the AFE.

RTUP-10

A 10GHz Low Phase Noise 0.13- μ m CMOS LC-VCO for Mixed Signal SoCs Using Noise Rejection Caged Inductors

A. Maxim, Maxim Inc., Austin, TX

Several coupled noise rejection techniques are proposed for LC oscillators operating in noisy mixed signal SoC environment. A metal guard ring around the LC-VCO achieved up to 10dB of coupled noise rejection. A compromise between cost, area and performance was achieved with a partial metal cage with no top plate and having graded lateral walls and a grid type bottom plate halo. Spur rejection in excess of 40dB with only a 10% penalty in inductor quality factor were achieved.

RTUP-11

All PMOS Wideband VCO with an Automatic Amplitude Controller for Multiband Multistandard Radios

Q. D. Bui, C. S. Park, School of Engineering, Information and Communications University (ICU)

A full PMOS, low phase noise, and wideband VCO with an automatic amplitude controller (AAC) is presented. The frequency band and tuning voltage are 2.78-3.78 GHz and 0-1.8 V, respectively. The measured phase noises at 1 MHz from carrier frequencies of 2.3, 3.24, and 3.77 GHz are -126.5, -125.0 and -122.7 dBc/Hz, respectively. With 1.8 V voltage supply, the current flowing into the VCO core varies from 4.9 mA to 5.7 mA. VCOs with/without an AAC were fabricated in TSMC 0.18 μ m CMOS technology.

RTUP-12

A 5.8-GHz VCO with Precision Gain Control

L. Jia, Y. B. Choi, W. G. Yeoh, Institute of Microelectronics, Singapore

We present a 5.8GHz LC VCO featuring over 300MHz tuning range while retaining VCO gain to as low as 45MHz/V. A modified frequency-tuning topology employing MOS varactors with virtual ground node bandswitching was adopted to set the appropriate frequency and to program K_{vco} to minimum. The VCO obtains an adjustable gain ranging from 45MHz/V to 106MHz/V in 20MHz/V-step. With minimum K_{vco} , phase noise improves by 6dB and goes to -115dBc/Hz at 1MHz offset from 5.98GHz, while dissipating 12.5mW power.

RTUP-13

Substrate Coupling Effect under Various Noise Injection Topologies in LC-Voltage Controlled Oscillator

S.-S. Wang, Y.-C. Wu, S. S. H. Hsu, C.-Y. Chan, Dept. of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C.

Impact of substrate noise coupling on a wideband VCO (5.6 to 7.5 GHz) was investigated using different noise injection topologies. Measured results indicated that IM2 increased by ~ 5 to 7 dB and IM3 by ~ 6 to 10 dB when the inductor guard ring floated. In addition, the noise at high frequencies still degraded the VCO performance even not injected directly to the substrate. The observed trends were modeled and explained by a simple physical-based resistive network successfully.

RTUP-14

A 45-to-60-GHz SiGe:C VCO for Millimeter-Wave Applications

J.-Y. Lee, S.-H. Lee, H. Kim, H.-K. Yu, ETRI, IT Convergence & Components Laboratory

A 45-60-GHz VCO is designed and fabricated using 0.25 μm SiGe:C BiCMOS process technology whose f_{max} is greater than 200 GHz. The VCO provides tuning range of 44.91-48.86 GHz when its bias current is 13 mA and of 58-60.38 GHz when a bias current of 7 mA flows into the VCO. Its phase noise is measured as -99 dBc/Hz from 48.86 GHz and -93 dBc/Hz from 60.32 GHz, at 10 MHz offset, respectively. The VCO shows moderate FOMs of 156 dBc at 60.32 GHz and 158 dBc at 48.86 GHz.

RTUP-15

5GHz Frequency Synthesizer With Auto Calibration Loop

M. Kim, K. Lee, Y. Kwon, J. Lim, T.J Park, IC design center, Samsung Electro-Mechanics

A 5-GHz frequency synthesizer for ZIGBEE (IEEE 802.15.4) was implemented. It consumes 13.5mW adopting CMOS Logic divider and robust VCO from process and temperature variation by body voltage control of current source. It incorporates an automatic capacitor-bank tuning loop to extend frequency tuning range. This synthesizer was fabricated in 0.18- μ m technology; it consumes 7.5mA at 1.8V and offers 100kHz-loop bandwidth and always -103dBc/Hz at an offset of 1MHz. The lock time is 30 μ s.

RTUP-16

Regenerative Frequency Divider with Synchronous Fractional Outputs

O. Momeni, K. Sengupta*, H. Hashemi, University of Southern California, *Indian Institute of Technology, Kharagpur

This paper presents an improvisation in tuned regenerative frequency divider topology that accomplishes division ratio of N with two synchronous fractional outputs suitable for frequency synthesis. A proof-of-concept divider with two synchronous output at 1/4 and 3/4 of the input frequency is designed in a 0.13 μ m CMOS technology. The implemented divider achieves a locking range of 5% at around 4GHz for an input power of 8dBm and a DC power consumption of 5mW from a 1V supply.

RTUP-17

A Highly Efficient Broadband (7-14 GHz) Monolithic Class E Power Amplifier for Space Based Radar

R. Tayrani, Raytheon Space & Airborne Systems

This paper describes the design and fabrication of a highly efficient broadband monolithic class-E power amplifier utilizing a new distributed class-E load topology. The amplifier maintains a simultaneous high PAE and output Power over 7.0 GHz of bandwidth. The HPA's measured performance shows a PAE range of (82% to 50%) and an output power of >25 dBm across 7-14 GHz. The new broadband load also renders the HPA to have an excellent spectrally pure frequency response demonstrated by its low AM and PM noise figures. A single 0.25 μ m x 720 μ m GaAs pHEMT device is used in this circuit.

RTUP-18

A 60-GHz CMOS Transmit/Receive Switch

C. M. Ta, S. Skafidas*, R. Evans*, University of Melbourne, *National ICT Australia

A single-pole double-throw (SPDT) transmit/receive switch (T/R switch) operating in the 57–66 GHz band is implemented on a 130-nm CMOS process. The switch exhibits an insertion loss from 4.5 dB to 5.8 dB, an isolation from 24.1 dB to 26 dB, a return loss at antenna port from -9.2 dB to -10.5 dB, and a return loss at Tx/Rx port below -15 dB for the frequency band. With a control voltage of 1.2 V the IP1dB of the switch is 4.1 dBm. The switch features fast switching speed with rise-time and fall-time of 400 ps and 360 ps, respectively. This is the first CMOS T/R switch designed for very short range radio in 60-GHz band.

RTUP-19

A 26 to 40GHz Wideband SiGe Balanced Power Amplifier IC

M. Chang, G.M. Rebeiz*, University of Michigan, Ann Arbor;
*University of California, San Diego

An integrated SiGe PA is presented for wideband applications covering 26 to 40GHz. No distributed amplifier or negative feedback techniques are employed to achieve wideband performance. The 42% fractional-bandwidth PA has a gain of 13dB and a saturated output power of 19.4dBm with 11.2% PAE from 32 to 33GHz. The output P1dB and Psat are greater than 15.5dBm and 17dBm, respectively, from 26 to 40GHz. The 1.83mm² chip consumes 525mW (375mA) from a 1.4V supply.

RTUP-20

Parasitic Capacitance Optimization of GaAs HBT Class E Power Amplifier for High Efficiency CDMA EER Transmitter

K.Y. Kim, J.H. Kim, S.M. Park, C.S. Park, Information and Communications University

A Class E PA for a CDMA EER transmitter is implemented with GaAs HBT technology. This paper demonstrates an efficiency improvement with a parasitic capacitance compensation circuit. In particular, the parasitic CBE affects a distortion of the input voltage signal and decreases the PA's efficiency. Using the compensation circuit, we obtain 7% collector efficiency improvement at a similar output power level. This PA exhibits output power of 29dBm and collector efficiency of 71% at 1.9GHz.

RTUP-21

A High Dynamic Range CMOS RF Power Amplifier with a Switchable Transformer for Polar Transmitters

Y. Kim, *B.-H. Ku, *C. Park, *D. H. Lee, *S. Hong, Samsung Electro-Mechanics Co., Ltd., *School of Electrical Engineering and Computer Science, KAIST

A fully integrated CMOS RF power amplifier for a 1.8 GHz band EDGE polar transmitter is presented. It is implemented with 0.18- μ m CMOS process. The output power is 33.4 ~ 33.5 dBm and the power added efficiency is 39 ~ 41 percent when the frequency varies from 1.71 to 1.91 GHz. The dynamic range is increased by 12 dB with the use of the proposed switchable transformer, which meets the EDGE dynamic range requirement of 37 dB when the supply voltage changes from 0.8 to 3.3 V.

RTUP-22

1.8-GHz CMOS Power Amplifier with Stage-Convertible Structure Using Differential Line Inductor

C. Park, D. H. Lee, J. Han, S.-H. Baek, Y. Kim*, and S. Hong, School of EECS, Korea Advanced Institute of Science and Technology (KAIST), Samsung Electro-Mechanics Co., Ltd.*

A 1.8-GHz power amplifier for a polar transmitter application is implemented using 0.18- μ m RF CMOS technology. Differential line inductor for differential circuit is proposed. The differential line inductor is used as low power matching network in the stage-convertible power amplifier in order to increase the efficiency at low output power region. The low power efficiency improvement for the power amplifier is 74 percent at an output power of 20 dBm.

RTUP-23

A 97.2 mW 1.8 GHz Low Power CMOS Transmitter for Mobile WiBro and WiMAX

H. Yoo, J. Kim*, T. W. Kim, M. Jeong, Y. Cho, , B. Kim, H. Shin*, B.-E. Kim, B.-K. Ko, Analog Devices Inc., Gyeonggi-do, Korea., * Kwangwoon University, Seoul, Korea.

To achieve high linearity performance with low power consumption, the transmitter employs linear trans conductor using a negative feedback amplifier and a current mirror amplifier is used for the transmitter mixer. In addition, multiple-gated transistor with two auxiliary transistors, and resistive source degeneration are used for the driver amplifier. With the proposed linearization techniques, a high linearity of 30.5 dBm OIP₃ is achieved with 97.2 mW power consumption, at 1.8 V supply voltage.

RTUP-24

Low-Capacitance SCR With Waffle Layout Structure for On-Chip ESD Protection in RF ICs

C.-Y. Lin, M.-D. Ker, Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University

Silicon-controlled rectifier (SCR) has been used as an effective on-chip ESD protection device in CMOS technology due to the highest ESD robustness. In this work, the waffle layout structure for SCR can achieve smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to ESD protection device can be reduced. The proposed waffle SCR with low parasitic capacitance is suitable for on-chip ESD protection in RF ICs.

RTUP-25

On the P+ Guard Ring Sizing Strategy to Shield Against Substrate Noise

S. Bronckers^{**}, G. Vandersteen^{**}, G. Van der Plas^{*}, Y. Rolain⁺, ^{*}IMEC, Belgium, ⁺ELEC, Vrije Universiteit Brussel, Belgium

Substrate noise coupling remains a major problem for a System on a Chip design. Guard rings are frequently used to shield the analog circuitry from the noisy digital circuits. In this paper measurements show that the isolation does not increase linearly with the guard ring width. It also shows that the effectiveness of the guard ring strongly depends on its ground connection. The effectiveness of the guard rings against substrate noise is demonstrated on a 5-7GHz LC Voltage Controlled Oscillator

RTUP-26

A Highly Integrated X-band Frequency Quadrupler MMIC

Y. Yamaguchi, T. Kaho, K. Uehara, NTT Corporation

A highly integrated X-band frequency quadruple MMIC using 3D-MMIC technology is presented. It consists of four amplifiers two doublers, and a 2-band elimination filter. These 7 circuits are integrated on only a 2.25 mm x 1.05 mm chip. The third and fifth harmonic components, which are spurious components nearest to the desired component, are well suppressed. The desired/undesired ratio is about 40 dB. The MMIC supplies +5 dBm of the fourth harmonic component at input power as low as -10 dBm.

RTUP-27**An Efficient Technique for Performance Analysis of a Receiver in the Presence of Calibration/ Compensation Algorithms**

C. Fernando, K. Muhammad, Texas Instruments

We present an efficient approach for evaluating the performance of a wireless receiver in the presence of calibration and/or compensation algorithms and various sources of measurement error. Noise figure and linearity performance of a receiver can be easily predicted

RTUP-29**Broadband Noise Modeling of SiGe HBT under Cryogenic Temperatures**

B. Banerjee, S. Venkataraman, C.-H. Lee*, J. Laskar, Georgia Institute of Technology, *Samsung RFIC Design Center.

In this paper, we present a detailed analysis and modeling of the broadband noise parameters for a 200 GHz SiGe HBT technology under cryogenic temperatures. A transit time based noise model is used to accurately predict the fundamental noise parameters a function of frequency and bias, using the measured Y-parameters of the device at 85K. Analytical equations are presented which represent the noise parameters as a function of device parameters and temperature.

MONDAY'S PANEL

12:00-13:15 PMA HCC - 313C

RFID: New Revolution or Remarketing of Existing Technologies in a New Package?

Moderator: Sayfe Kiaei, Arizona State University

Panelists: Reza Rofougaran, Broadcom Inc.; Ganesh K. Balachandran, Texas Instruments; Mitsuo Usami, Hitachi, Ltd.; Frank Mau-Chung Chang, UCLA; Robert Plana, LAASCNRS; Issy. Kipnis, Intel; Scott Chiu, Intel; John Adams, Freescale Inc.

Sponsor: RFIC

This panel will focus on the development, architecture, applications, security, and system-level issues of RFIDs. New RFID technologies have the potential to revolutionize business processes and help create innovative end-user applications. This panel will discuss the future of RFID technologies and the potential impacts of this technology:

- What is unique and new in RFID?
- What is different from ZIGBEE and other 802.11 low-power solutions?
- Will it take the Bluetooth path?
- Is it a marketing hype or a reality?
- What are the RF-design challenges here?

TUESDAY'S PANELS

12:00-13:15 PTUA HCC - 313C

CMOS Millimeter-Wave MMIC: Real or Bubble?

Moderator: Hiroshi Kondoh, Hitachi Ltd.

Panelists: Sorin Voinigescu, University of Toronto; Rudolf Lachner, Infineon Technology; Huei Wang, National Taiwan University; Kenjiro Nishikawa, NTT; Tuneo Tokumitsu, Eudyna Devices; Herbert Zirath, Chalmers Univ. of Technology; Ali M. Niknejad, UC Berkeley

Sponsor: RFIC

CMOS would be the most promising device for millimeter applications. But, when will the millimeter-wave CMOS IC be a real product? What kinds of applications are expected? The panel will discuss the pros and cons of CMOS and other devices, and will show these technical trends/market forecast.

TUESDAY'S PANELS (continued)

12:00-13:15 PTUB HCC - 316C

Your GaAs Foundry and the Future: Anyone Have Issues? Of Course!

Moderators: Brad Nelson, Sirenza Microdevices; Paul Blount, Custom MMIC Design Services

Panelists: Wing Yau, Global Communication Semiconductor; Bob Donahue, Win Semiconductor; Phillippe Labasse, United Monolithic Semiconductors; Mike Peters, TriQuint Semiconductor; Marc Rocchi, Ommic; David Smith, Filtronic

Sponsor: IMS

Come ask the foundries how they plan to solve your problems. This panel session will address key issues facing GaAs foundries and their customers today and in the future: performance, reducing cost, quality control, emerging markets, second sourcing, consolidation, disruptive technologies.

WEDNESDAY'S PANELS

12:00-13:15 PWA HCC - 313C

Is GaN Ready for Prime Time?

Moderator: Mark Rosker, DARPA

12:00-13:15 PWB HCC - 316C

Will RF-MEMS Make the Commercial Leap?

Moderators: Scott Barker, University of Virginia
Gabriel Rebeiz, University of California San Diego

12:00-13:15 PWC HCC - 317A

Grant Opportunities at the National Science Foundation

Moderators: Leda Lunaradi, NSF
Don Senich, NSF

THURSDAY'S PANELS

10:10 - 11:50 PTHA HCC - 317A

Career Development: Giving Your Career A Never-Ending Boost Chair:

Moderators: S. Pacheco, Freescale Semiconductor
R. Henderson, Freescale Semiconductor

12:00 - 13:15 PTHB HCC - 313C

THz Electronics for the 21st Century

Moderator: Richard Lai, NGST

12:00-13:15 PTHC HCC - 316C

RF Techniques for Signal Integrity Engineering

Moderator: Ashok Bindra, RF Design Editor

IEEE and MTT-S REGISTRATION

IEEE

The IEEE is a nonprofit, professional association with more than 367,000 members (including 73,000 students) in over 150 countries. This global organization helps support the development and application of technology and science around the world.

MTT-S

The IEEE Microwave Theory and Techniques Society (MTT-S) is a transnational society with more than 9,000 members and 80 chapters worldwide.

Join the IEEE and MTT-S

To join the IEEE or renew your membership, please visit, email, or call: www.ieee.org/services/join/new.membership@ieee.org 1-800-678-IEEE Attendees who join the IEEE for \$80.50 and MTT-S for \$7.00 before the Symposium will save \$185 on their registration fee. The price of an IEEE/MTT-S membership more than pays for itself! Half-year rates apply to new members only. New applications received between 1 March 2007 and 15 August 2007 will automatically be processed for half-year membership. An exception is made if the applicant specifically requests their application be processed for the full year.

ADVANCE REGISTRATION INFORMATION

Advance Registration

Please follow these instructions for completing the Advance Registration Form on the center page. Advance registration rates are valid until the deadlines shown on the form and are approximately 30% lower than the on-site fees. Registration is required for all attendees, including session chairs and presenters. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and Exhibition Hall. This form is not used for guest tour registration, which is described elsewhere in this Program Book. Each registrant must submit a separate form with payment. Registration by telephone is not available, but for handicap, special needs, or information only, call 1-781-769-9750.

Methods of Registration

Individuals can register online, by FAX, or by mail. Those registering by mail should send their form in early enough to ensure the application is received by the deadline, otherwise on-site fees will be charged. If the registration is sent by FAX, do not send it by mail. Additional items can be added on site after advance registration.

Personal Information

For phone numbers outside the USA, please include a country code. If you would like to receive information by email from the IEEE, MTT-S, or microwave companies, mark the appropriate boxes. An optional complimentary badge for one guest allows access to the Hospitality Suite, Plenary Session, and Exhibition Hall, but does not allow access to technical sessions, Workshops, and Short Courses.

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check-in will be charged the nonmember rate. If you are not a member and wish to take advantage of the member rates, call 1-800-678-IEEE or visit www.ieee.org/services/join prior to registering.

Symposia

Microwave Week hosts three symposia: the International Microwave Symposium (IMS), the RFIC Symposium, and the ARFTG Conference. Select the conferences you wish to attend. Students, retirees and IEEE Life Members receive a discount on registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full-time student carrying a course load of at least nine credit hours.

- IMS technical sessions are held on Tuesday, Wednesday, and Thursday. Registration includes continental breakfast, admission to exhibits, abstract books, and a CD-ROM.

- RFIC technical sessions are held on Monday and Tuesday. Registration includes continental breakfast, admission to the RFIC Reception and exhibits, a digest, and a CD-ROM.
- ARFTG technical sessions are held on Friday. Registration includes breakfast, lunch, a CD-ROM, and admission to the ARFTG exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE members.
- Exhibits: Microwave Week hosts the largest exhibition of its kind with over 400 companies. Exhibit-only registration is available on-site for \$20. Extra CD-ROMs and Digests
Additional CD-ROMs and digests are available for purchase and pickup at the conference. After the symposium, digests and CDROMs will be available for purchase from IEEE.

Awards Banquet

The MTT-S Awards Banquet will be held on Wednesday from 19:30 to 22:00 at the Hilton Mid-Pacific Conference Center Coral Ballroom 4. The evening will include a fine dinner, awards presentation, and entertainment. Major Society awards will be presented.

Box Lunches

Optional box lunches are available for purchase by all attendees, but are especially convenient for those attending the Panel Sessions or Exhibition Hall during lunchtime, since dining alternatives in the vicinity of the Convention Center are limited. Purchase now, because on-site pricing will be higher. Sorry, but no refunds are possible since these lunches are preordered.

Workshops and Short Courses

The Workshop fee includes a CD-ROM and speakers' notes for that workshop. The Short-Course fee includes all instructor-provided material for that course. Full-day and morning workshops and short courses include continental breakfast, a box lunch, and refreshment breaks. Afternoon workshops include a box lunch and afternoon refreshments. The All-Workshop CD-ROM fee includes material for all workshops on one CD-ROM but does not include admission to any workshops.

Remittance

Individual remittance must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on a U.S. bank, traveler's check, international money order, or credit card (VISA, MasterCard, or American Express only). Personal checks must be encoded at the bottom with the bank, account, and check number. Bank drafts, wire transfers, cash, and purchase orders are unacceptable and will be returned. Make checks and money orders payable to "IEEE/MTT-S." Written requests for refunds will be honored if received by 4 May 2007. See Page 86 for the full refund policy.

ON-SITE REGISTRATION INFORMATION

On-Site Registration

On-site registration for all Microwave Week Events will be held at the Hawaii Convention Center.

Registration hours are:

Day	Time
Saturday, 2 June 2007	14:00-18:00
Sunday, 3 June 2007	07:00-18:00
Monday, 4 June 2007	07:00-17:00
Tuesday, 5 June 2007	07:00-17:00
Wednesday, 6 June 2007	07:00-17:00
Thursday, 7 June 2007	07:00-15:00
Friday, 8 June 2007	07:00-09:00

Exhibition-Only Registration

Exhibition-only registration is available on-site for \$20.

Guest Tour Registration

Registration for guest tours are handled at the Hospitality Suites and in the Hawaii Convention Center Lobby. Refer to the Guest Program section of this Program Book for further details.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to technical sessions and exhibits. Digests are not included. The Press Room is located in HCC 328 on Tuesday through Thursday.

ARFTG Registration

Late on-site ARFTG registration will be available at the Hilton Mid-Pacific Conference Center on Friday from 07:00 to 11:00. If at all possible, please preregister earlier in the week to reduce the on-site workload.

On-site registration fees are as follows:

Event	Member	Nonmember
IMS sessions	\$495 (\$75) [†]	\$740 (\$155)
IMS sessions (no CD-ROM)	\$425	\$630
Single-day registration	\$260	\$360
RFIC sessions	\$250	\$375
RFIC Reception only	\$60	\$80
ARFTG sessions	\$260 (\$165)	\$400 (\$165)
IMS and ARFTG CD	\$70	\$140
RFIC Digest	\$70	\$130
RFIC CD-ROM	\$70	\$130
Box lunches (per day)	\$25	\$25
Awards Banquet	\$90	\$90
Workshops (full day)	\$200 (\$135)	\$300 (\$135)
Workshops (half day)	\$150 (\$100)	\$225 (\$100)
All-Workshop CD-ROM	\$240 (\$115)	\$350 (\$115)
ARFTG Conference		
Compendium CD-ROM	\$105	\$140
ARFTG Workshop		
Compendium CD-ROM	\$70	\$105
Exhibit-only pass	\$20	\$20

[†]Student, retiree, and IEEE Life Member prices are shown in parentheses.

Refund Policy

Written requests received by 4 May 2007 will be honored. Refund requests postmarked after this date and on-site refunds will be granted only if an event is cancelled. This policy applies to registrations for the symposium sessions, Workshops, Short Courses, digests, extra CD-ROMs, Awards Banquet, and box lunches. Please state the preregistrant's name and provide a mailing address for the refund check. If registration was paid by credit card, the refund will be made through an account credit. An account number must be provided if the initial registration was done on-line. Address your requests to:

MTT-S Registration
685 Canton St.
Norwood, MA USA 02062-2608

UNITED STATES VISA ADVISORY

The U.S. has updated its visa policies to increase security. It will likely take longer to get a visa than it used to, and applicants will find that a few new security measures have been put into place. For details that may apply specifically to your country, see information posted by your nearest U.S. Consulate or Embassy.

Citizens of certain countries, traveling for visitor visa purposes for 90 days or less and who meet all the requirements, can travel to the United States for tourism or business under the Visa Waiver Program (VWP).

Visa Waiver Program

Currently, the 27 countries shown below participate in the VWP. Some citizens of Canada and Bermuda do not need a visa to visit the U.S.

Andorra	Australia	Austria	Belgium
Brunei	Denmark	Finland	France
Germany	Iceland	Ireland	Italy
Japan	Leichtenstein	Luxembourg	Monaco
The Netherlands	New Zealand	Norway	Portugal
San Marino	Singapore	Slovenia	Spain
Sweden	Switzerland		United Kingdom

Passports

Since October 2004 visa waiver travelers from all VWP countries must present a machine-readable passport at the U.S. port of entry.

A passport with a validity date at least six months beyond the applicant's intended period of stay in the U.S. is required.

Recommendations

To avoid frustration and disappointment:

- Advance planning by travelers is essential. Review your visa status and find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your departure date. Contact your nearest U.S. embassy or consulate for a current time estimate and recommendations.

Visa Letters

A visa support letter may be provided for authors and registered attendees. Further, spouses requiring visa assistance must be registered for an IMS/RFIC Guest Program event.

WORKSHOP INTRODUCTION

Workshops and Short Courses are offered on Sunday, Monday, and Friday and are distinguished by the following features:

- Advanced-level Workshops (designated as WSA, WSB, etc.) present the state of the art to specialists who are already experienced in the topic area.
- Tutorial-level Workshops (TSA, TSB, etc.) are targeted toward educating attendees in new areas of microwave technology, reviewing material that is primarily a revision of previously published information
- Short Courses (CSA, CSB, etc.) are offered by a well-coordinated team of two experts following a detailed course outline, providing a coherent tutorial presentation of a single topic to non-specialists. Each participant earns IEEE continuing education units.

All Workshops and Short Courses will be held at the Hawaii Convention Center. Specific room assignments will be announced at check-in.

A detailed description of RFIC Sponsored Workshops and Short Courses on Sunday follow. A listing of IMS Workshops Titles on Sunday, Monday, and Friday are included for information.

Sunday RFIC Sponsored Workshops and Short Courses

08:00-17:00 WSA

Architectural Design and System Verification for Wireless SoC – Nice to Have or a Real Necessity?

Topics and Speakers:

- Best Practices for Adopting Model-Based Design into Wireless SoC Development Flow, C.Warwick, The Mathworks
- Analog-on-Top Verification of AMS-RF Applications, J. Hartung, Cadence
- Automated Design Validation Flow for Mixed-Signal SoCs, T. Tarim and O. Eliezer, Texas Instruments
- Study of Existing Methods for Wireless System Design and Propose a New Method for Top-down and Bottom-up Design in RF, Y. Miyahara, Panasonic R & D Company of America
- System-Level Verification from RF-Level Design, S.Wedge, Synopsys
- Architectural Design and System Verification for Wireless SoC, a Must for Multimode Cellular Transceivers, D.Schwarz, Freescale Semiconductor
- Architectural Design and System Verification for Wireless SoC - Nice to Have or a Real Necessity? M.Barnasconi, NXP Semiconductors
- A Top Down Design Methodology for Mixed-Signal Integrated Circuits using C++ Behavioral Modeling, M. Perrott, MIT-EECS

Organizers: J. Niehof, NXP Semiconductors; M. Barnasconi, NXP Semiconductors

Sponsor: RFIC

As more and more digital signal processing is included in the RF pipe, not only for modulation and demodulation purposes, but also to facilitate digital calibration, testing and configuration, an overall system-level design approach at architecture level is essential. Furthermore, verification of the complete embedded system solution, including RF and mixed-signal circuitry, is becoming recognized as an essential step in the design release process before committing to tape-out. This workshop brings together representatives from the RF semiconductor and EDA industries to discuss current and future trends in architectural design and system verification that successfully address these challenges.

08:00–17:00 WSB

Wireless Reconfigurable Terminals: Adaptive Analog Circuits or Digital RF Processing?

Topics and Speakers:

- Reconfigurable Si RF Receiver Front-Ends for Multistandard Radios, M. Brandolini, Broadcom Corporation
- Reconfigurable Analog Baseband Circuit Design, O.K. Shanaa, Maxim Integrated Products
- Digital RF Processing for Wireless Receivers, K. Muhammad, Texas Instruments
- Digital RF Processing for Wireless Transmitters, O. Eliezer, Texas Instruments
- Reconfigurable Transmitters and Power Amplifiers, L. Larson, UC San Diego
- Polar Transmitters for Reconfigurable Radios, E. McCune, Panasonic Emerging Advanced RF Laboratory
- Reconfigurable ADCs / DACs for Multimode Terminals, K. Gulati, BitWave Semiconductor Inc
- Reconfigurable VCOs and Synthesizers, A. Gnudi, University of Bologna

Organizers: W. Y. Ali-Ahmad, American University of Beirut;
O.K.Shanaa, Maxim Integrated Products

Sponsor: RFIC

“Life goes wireless!” This motto for the 21st century is pushing the evolution of new wireless devices, which confirm to multiwireless standards and operate over multifrequency bands. This workshop will review current adaptivity design concepts for reconfigurable RF and analog base band integrated front-ends. In addition, it will present new Digital RF Processing (DRP) techniques for wireless transceivers, which move the radio reconfigurability concept to the digital domain.

13:00–17:00 WSC

Optimum CMOS Integrated LNA Design Techniques for

Handsets

Topics and Speakers:

- Design of CMOS Receiver LNAs, J.Long, Delft University of Technology
- State of the Art Techniques for High Linearity Integrated CMOS Low Noise Amplifiers, V. Aparin, Qualcomm
- Modulated-Signal Distortion Measurements to Support Nonlinear Circuit Simulation, K. Remley, NIST
- Device Modeling and Technology Parameters Affecting LNA Performance, J.Pekarik, IBM
- Interface, Co-Integration and Stability Aspects of Modern CMOS LNA Designs, T. McKay, RFMD
- Case Studies of Three Cellular LNA Designs in 90nm CMOS, D. Griffith and S. Pennisi, Texas Instruments

Organizers: T. McKay, RFMD; J. Pekarik, IBM; L. Reynolds, RFMD

Sponsor: RFIC

This workshop will cover new techniques specific to CMOS LNA design for handsets in existing and emerging standards bands in the 800MHz to 6GHz frequency range. Focus on exploiting CMOS technology, with learning from 0.25 μm through 90 nm, emphasizing 90 nm and below where design iteration is prohibitive and excellence is demanded. By expounding on issues such as source mismatch, stability, nonlinear simulation accuracy, manufacturability, increased confidence in new techniques is developed.

08:00-17:00 WSD

Nanoscale RFIC Design Challenges and Foundry Solutions

Topics and Speakers:

- Advanced Nanoscale RFCMOS Foundry Technology Challenges and Solutions, J. Chern, S. Liu, TSMC
- Nanoscale RFCMOS Foundry Technologies and Design Support, A. Yen, UMC
- Design Challenge of ESD Protection, RF I/O, and Low Voltage Consideration in Mixed Process Node Deep Submicron and Nanometer CMOS Technologies, P. Ouyang, T. Yu, F. Lo, I.C. Chen and L.W. Yang, SMIC, R. Huang, H. Liao, PKU, Beijing, Y. Cheng, SHRIME, Peking U., A. Wang, Illinois Institute of Technology
- Foundry Solutions for Next-Generation RFIC Design, M. Racanelli, Jazz Semiconductor
- Topics in Wireless RFIC Design Methodology Going to Submicron Semiconductor Processes, R. A. Mullen, Cadence Design System

- RF SiP Solution and Challenges, C. T. Chiu, ASE Corp.
- Enhancing Overall Nanoscale RF CMOS System Performance with the Right Packaging Solution, N. Karim, Amkor Technology
- CMOS Scaling Impacts to RF/Mixed-Signal Circuit Design, M.C.Frank Chang,UCLA
- CMOS RF Transceivers for 5-GHz Broadband Wireless Access, S. S. Lu, H. C. Chen,National Taiwan U.
- Mixed-Signal Design Techniques for Deep-Submicron CMOS Single-Chip Receiver SOCs, A. Maxim and R. Poorfard, Silicon Laboratories
- Device Variability of Nanoscale RF CMOS Circuits and its System Mitigation,B. Staszewski and O.Eliezer, Texas Instruments Inc.

Organizers: L. W. Yang, SMIC; K. C. Wang, UMC; J. Lin, University of Florida

Sponsors: RFIC, MTT-9

Semiconductor foundries have been playing an increasingly important role in IC industry. RFCMOS technologies are mostly based on the processes for digital applications. The traditional RF design techniques are limited by transistor leakage current, device mismatches, passive components, ESD protection, noise and substrate modeling. This workshop addresses these limitations and solutions.

08:00-12:00 WSH

UWB Radio: From Building Block to SoC

Topics and Speakers:

- Use of Cognitive Radio Techniques for OFDM Ultra-Wideband Coexistence with WiMAX, J. Lansford, Alereon, Inc.
- RF/Mixed-Signal IC Design for UWB OFDM Systems, S. Raman, Virginia Polytechnic Institute and State University.
- Design Strategies for CMOS UWB Radios, A. H-C. Kang, Realtek
- ESD Protection for Wideband RF CMOS Circuits – Challenges, Options and Trade-offs, N. Iyer, Silterra Malaysia Sdn Bhd
- Front-end Amplifier Design for Ultra-Wideband Systems, R. Gharpurey, University of Texas at Austin
- C-Wave UWB Chipsets, R. Sengottalyan, Pulse-Link

Organizers: A.Wang, Illinois Institute of Technology; L.Yang, SMIC; Y.Zhou, The Chinese Academy of Sciences

Sponsor: RFIC

This workshop focuses on advances in developing Si-based ultra-wideband (UWB) radio integrated circuit systems. Topics covers from front-end blocks to UWB SoCs, including, low noise amplifiers, pulse generators, mixers, multipliers, ADC, transmitters, receivers, timing, digital baseband, MAC, etc. Attendees will be exposed to critical design issues and tricks related to UWB SoC designs.

08:00-12:00 WSJ

RFID

Topics and Speakers:

- Introduction to RFID and Passive Tag ICs, N.Camilleri, Alien Technology
- Passive UHF RFID CMOS Tag IC Using Ferroelectric RAM Technology, S.Masui and T. Ninomiya, Fujitsu
- Challenges and Design of UHF RFID Reader Integrated Transceivers, I.Kipnis, Intel Corporation
- Trends for Mobile RFID Reader SoCs, Developed by Korean ASIC Companies, J.S.Park, Kookmin University
- Fully Integrated UHF RFID Systems for Near-field and Far-field Applications, R.Rofougaran and M.Rofougaran, Broadcom
- Reader Chipset for UHF RFID, M. O'Neal, WJ Communications

Organizer: N.Camilleri, Alien Technology

Sponsor: RFIC

RFID technology has come a long way in the last decade. RFIC implementations have enabled very small RFID tag chips that work at 13, 900, and 2400 MHz. Reader technology has also come a long way and is currently morphing from several discrete implementations to custom integrated solutions. The workshop will provide an introduction to RFID and then will dive into the tradeoffs and techniques that one has to do to implement small tag ICs and high performance reader chip sets.

13:00-17:00 WSL

Software Defined Radio to Cognitive Radio

Topics and Speakers:

- Software Defined Radio Transceiver SOC approach, A. Abidi, UCLA
- Software Defined Radio Transceiver SIP approach, L. Larson, UCSD
- Industrial Software Defined Radio Transceiver example, R. B. Staszewski, Texas Instruments
- Towards Cognitive Radio, T. Martin, Science & Technology Associates

Organizers: D. Belot, ST Microelectronics; J. B. Begueret, IXLLab

Sponsor: RFIC

This workshop will focus on new design of radio architectures (circuits and systems) dedicated to Software Defined Radio (SDR) and Cognitive Radio (CR), which is the main challenge for the next generation of RF transceivers. In order to frame the workshop we have extracted two definitions of what are SDR and CR. SDR is a radio that includes a transmitter in which the operating parameters of frequency range, modulation type or maximum radiated power (either radiated or conducted), or the circumstances under which the transmitter operates can be altered by making a change in software without making any changes to hardware components that affect the RF emission. Extracted from US FCC Cognitive Radio Report and Order, CR is a radio or system that senses and is aware of its operational environment and can be trained to dynamically and autonomously adjust its radio operating parameters accordingly.

13:00–17:00 WSN Millimeter-Wave/Quasi-Millimeter-Wave Highly Integrated Circuits

Topics and Speakers:

- Silicon Technology, Circuits, Packages, and Systems for 60–100GHz Communications and Radar Systems, B. Floyd, IBM
- Highly Integrated GaAs MMICs using Three-dimensional MMIC Technology, Y. Yamaguchi, NTT Corporation
- SoP Integration of 60GHz Radio, C.S.Park, Information and Communications University
- CMOS Millimeter-wave Frequency Sources, C. Cao and K. K. Oh, University of Florida

Organizers: T.Nakagawa, NTT Corporation; N. Suematsu, Mitsubishi Electric Corp.

Sponsor: RFIC

There are many RF system-on-chip devices in which the operating frequencies are below 6GHz. Because millimeter-wave and quasi-millimeter-wave integrated circuits are traditionally implemented using compound semiconductors such as GaAs or InP, the integration scale is limited. However, recent progress in device technology can overcome the problem. This workshop will focus on highly integrated circuits whose operating frequency is over 20GHz.

08:00-12:00 WSO**Silicon BiCMOS and CMOS PA from RF to mmWave***Topics and Speakers:*

- CMOS Devices for Power Amplifiers, J.D. Alamo, MIT
- CMOS Power Amplifiers for mmWave Applications, A. Niknejad, University of Berkeley
- RF CMOS PA for Cellular and WLAN Applications, D. Masliah, Acco Company
- CMOS Transmitter Combining Amplitude Modulator and Power Amplifier, J. Loraine, RadioSis, Limited

Organizers: D. Belot, STMicroelectronics; E. Kerherv, IXL Lab; Y. Deval, IXL Lab

Sponsor: RFIC

This workshop will deal with the most recent developments of CMOS or BiCMOS power amplifiers for cellular, LAN, PAN, satellite and radar applications. The frequency range covered is from 1GHz up to 100GHz. The presenters will compare new BiCMOS or CMOS circuits and/or devices with existing ones in technologies brought into play presently (i.e., InP, GaAs). The presenters will be balanced with academic and industrial affiliations.

13:00-17:00 WSP**Integrated Broadband Tuners for Satellite and Terrestrial Applications***Topics and Speakers:*

- Silicon RFICs for Direct Broadcast Satellite Communications, W. Gao, Conexant Systems
- Multiband Multimode Mobile TV Tuner in CMOS, B. Kim, Analog Devices Inc.
- Frequency Synthesizer Architectures for Broadband Tuners: Ring Oscillator versus LC Oscillator and Low-IF versus Zero-IF Receivers, A. Maxim, Silicon Laboratories
- SiGe IC Design for Satellite Microwave Front-Ends, C. Vaucher, NXP Semiconductors

Organizers: B. Bakaloglu, Arizona State University; S. Kiaei, Arizona State University; Y. Deval, University of Bordeaux

Sponsor: RFIC

Integrated broadband tuners have several design challenges due to wide tuning range, linearity under several blocker channels, dynamic range and harmonic mixing of blocker channels. This workshop will focus on architectures and circuits for addressing several design challenges associated with integrated broadband tuners for terrestrial, cable and satellite applications.

08:00-17:00 TSA**RFIC Circuit and System Design Tutorial Topics and Speakers:**

- On-chip Inductor and Transformer Modeling, D.K. Shaeffer, Beceem Communications
- RF CMOS IC Simulation Improvements and New Industry Standard MOSFET and CMOS Varactor Models, J. Victory, Jazz Semiconductor
- Transmitter Architectures and Circuits, J.C.Rudell, Intel Corporation
- Receivers: Architectures and Circuit Design, D. Ozis, Telegent Systems
- A/D Converters for Wireless Communication in Nanometer CMOS, Y. Chiu, University of Illinois
- Piezoelectric Contour-Mode Vibrating RFMEMS, G. Piazza, University of Pennsylvania
- Frequency Synthesis for Wireless Systems, W. Khalil, Intel Corporation
- All-Digital TX and Discrete-Time RX, R. Staszewski, Texas Instruments

Organizer: J. C. Rudell, Intel Corporation; D. K. Shaeffer, Beceem Communications

Sponsor: RFIC

This workshop will begin by covering the basics of transceiver design. Topics will range from CMOS device and passive component modeling to wireless building block design to the realization of full transceiver systems on a chip. High integration transmitters, receivers, and synthesizers as well as newer digital transceivers systems will be discussed. In general, this tutorial heavily emphasizes CMOS circuit design and high integration radios for common commercial standards including cellular and Wireless LAN.

08:00-17:00 TSB**Analog and High-Speed Circuit Design Solutions for Nano RFCMOS***Topics and Speakers:*

- RFIC Case Study, D. Schmidt, Intel Corporation
- Challenges for Nanoscale Transceivers Embedded in Highly Complex SoC's, A. Hanke, Infineon Technologies
- Digital RF Processor (DRP™) Wireless SoC in Nano RF CMOS, S. Pennisi, Texas Instruments
- Silicon – Package Co-Design, N. Karim, Amkor
- Overview of 90 nm Challenges, A. Yen, UMC Corporation
- On-chip Transformer Cascode Circuit Design Techniques, D. Huang, UCLA
- EDA Design Solutions for Nano CMOS, D. Wu, Ansoft Corporation
- Nano-scale CMOS Computer Hands-on Session, D. Wu, Ansoft Corporation

Organizer: L. I. Williams, Ansoft Corporation; Y. Cheng, Siliconlinx Inc.

Sponsor: RFIC

Better performance and integration motivates RF designers to implement circuits at the 90-nm node and below. This scaling enables greater performance but introduces significant risks for designing and fabricating RF, analog, and high-speed circuits.

This workshop provides practical design solutions to challenges of nanoscale CMOS by leading experts in IC design, packaging, foundry, and EDA. Issues such as low-threshold voltage, noise, high leakage, high variability, and DFM will be explored. A unique computer hands-on session allows attendees to simulate many of the concepts covered.

Sunday IMS Sponsored Workshops and Short Courses

08:00-17:00 WSE

System-in-Package Technologies for Cost, Size, and Performance

08:00-17:00 WSF

Advances in WiMAX RF Technology

08:00-17:00 WSG

Solid-State Power Invades the Tube Realm

13:00-17:00 WSI

Advances in Mixer Design for UWB Transceivers

13:00-17:00 WSK

Emerging RFID and Wireless Sensors: Technologies and Applications

08:00-12:00 WSM

24GHz ISM-Band Communications

08:00-17:00 TSC

Tutorial Workshop on RF and Microwave Filter Design

08:00-12:00 TSD

SDR and Cognitive Radio – The Need for Reconfigurable RF Front-Ends

08:00-17:00 CSA

Micro Coaxial Lines: Theory, Design, and CEM Lab

08:00-12:00 CSB

Galileo – Europe's Share for a Global Navigation Satellite Service

Monday IMS Sponsored Workshops and Short Courses

08:00-17:00 WMA

Advances in Active Device Characterization and Modeling for RF and Microwave

08:00-17:00 WMB

On-Chip/Off-Chip DC ,RF, and Microwave Measurement Modules for RFIC, SoC, and SiP Self Characterization, SelfTest, SelfDebug, and Diagnosis

08:00-17:00 WMC

High-Speed Signal Integrity

08:00-17:00 WMD

Emerging Packaging Technology and Applications at Millimeter-Wave Frequencies

08:00-17:00 WME

Hig-Q RF MEMS Tunable Filters

08:00-17:00 WMF

Theory and Design of Phase Locked Loops

08:00-17:00 WMG

Challenges of High Power Device Characterization and Modeling

08:00-17:00 WMH

High Power Issues of Microwave Filter Design and Realization

08:00-12:00 WMI

Noise in Nonlinear Circuits: Theory,Modeling, and Measurement Techniques

08:00-17:00 WMD

Emerging Packaging Technology and Applications at Millimeter-Wave Frequencies

08:00-17:00 WME

High-QRF MEMS Tunable Filters

08:00-17:00 WMF

Theory and Design of Phase Locked Loops

08:00-17:00 WMG

Challenges of High Power Device Characterization and Modeling

08:00-17:00 WMH

High Power Issues of Microwave Filer Design and Realization

08:00-12:00 WMI

Noise in Nonlinear Circuits: Theory, Modeling, and Measurements Techniques

13:00-17:00 WMJ

Will Wide Band-Gap Power Transistors Render Silicon Power Transistors Obsolete?

08:00-12:00 WMK

Ultrafast Analog-to-Digital (A/D) Conversion

08:00-17:00 TMA

High-Frequency Characterization of Printed-Circuit Board Materials

08:00-17:00 TMB

Practical Analysis, Stabilization, and Exploitation of Nonlinear Dynamics in RF, Microwave, and Optical Circuits

08:00-12:00 TMC

How to Do Business in Far East

13:00-17:00 TMD

Novel Materials for RF MEMS

08:00-12:00 CMA

RFID – Design of Integrated Passive Transponders

08:00-17:00 CMB

Millimeter-Wave and THz Electromagnetics, Components, and Systems

Friday IMS Sponsored Workshops and Short Courses

08:00-17:00 WFA

Reconfigurable and Smart Antennas

08:00-17:00 WFB

Recent Advances in Electromagnetic Metamaterials: Theory, Computation, and Applications

08:00-17:00 WFC

Low-Cost, Integrated Automotive and Industrial Radar Sensors

08:00-17:00 WFD

Advances in Imaging Radar Technology

08:00-17:00 WFE

Terahertz Device Characterization and Security Applications

08:00-12:00 WFF

Wireless Local Positioning

13:00-17:00 WFG

Wireless Power Transmission for Space Solar Power Generation

13:00-17:00 WFH

Miniature, Electronically Tuned Filter Technology

08:00-12:00 WFI

GaN Device and Circuit Reliability

08:00-12:00 TFA

Microwave and Millimeter-Wave Packaging and Manufacturing 202

13:00-17:00 TFB

Multidomain Physics Modeling of MEMS and NEMS

08:00-12:00 TFC

Nanoelectronic Devices: RF Characterization, Modeling, and Applications

08:00-17:00 CFA

Applications of Artificial Neural Networks to RF and Microwave Design

08:00-17:00 CFB

Time-Domain Electromagnetic Simulators

08:00-12:00 CFC

RF Linear Accelerators

08:00-17:00 CFD

LTCC for Micro- and Millimeter-Wave Applications

TRANSPORTATION

Airport Transportation

The Honolulu International Airport (HNL) is on the south shore of Oahu, just west of Honolulu's central metropolitan center. It is approximately 12km from the Hawaii Convention Center (HCC) and is approximately 30 minutes away depending on traffic.

Taxi

Taxi service is available on the center median fronting the terminal baggage claim areas. The fare from the airport to Waikiki during for periods outside of rush hour is \$25–\$35.

24-Hour Bus Service

Air-conditioned bus service operated by Roberts Hawaii is available 24 hours a day and departs from the airport approximately every 20 minutes. Fares are \$9 one way, \$15 roundtrip. Call 1-808-954-8652 for information or visit www.robertshawaii.com/hat.htm.

Prearranged Ground Transportation

There are numerous shuttle companies available on a prearranged basis. Company names and telephone numbers are available at www.hawaii.gov/dot/airports/hnl/hnl_ground_trans.htm.

Rental Cars

Major rental car companies at HNL include Hertz, Alamo, Dollar, Enterprise, Budget, and Thrifty. Please visit their respective web sites for further information.

Hotel to HCC Bus Service

Complimentary bus service to and from HCC will be provided for those reserving their hotel room through the IMS 2007Housing Bureau. The pick-up and drop off zones are located at:

- Zone 1: Hilton Hawaiian Village, Doubletree
- Zone 2: Hawaii Prince
- Zone 3: Sheraton, Royal Hawaiian, Ohana Waikiki
- Zone 4: Hyatt, Princess Kaiulani, Ohana West

City Bus

Public transportation is available for \$2 via the city bus service, "The Bus." Drop-off and pick-up points, as well as hours of operation, can be found at www.thebus.org.

Convention Center Parking

There are 690 parking stalls at HCC. The cost is \$5 per entry. A \$25 parking card, valid for 30 days, is available for purchase (cash only) from the HCC Security

SOCIAL EVENTS

The Hilton Mid-Pacific Conference Center is abbreviated in the text below as Hilton MPCC.

Sunday, 3 June **19:00-21:00**
RFIC Reception **HCC – Rooftop Garden**

Immediately following the RFIC Plenary Session is the RFIC Reception on the Rooftop Garden of the Hawaii Convention Center. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

Monday, 4 June **18:00-20:00**
Microwave Journal Reception **HCC – Rooftop Garden**

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by Microwave Journal. The venue is the 2.5 acre landscaped roof-top garden atop the Hawaii Convention Center.

Tuesday, 5 June **18:00-20:00**
Women in Microwaves Reception **Hilton Village Green**

Surrounded by lush tropical gardens, gentle waterfalls, and an adjacent koi pond, the beautiful Village Green, centrally located between the Tapa Tower and Main Lobby at the Hilton Hawaiian Village, is the perfect venue for celebrating the diversity of MTT-S.

Tuesday, 5 June **19:00-21:00**
Student Reception **Hilton Kalia Tower Pool**

All students are invited to socialize poolside in a relaxed and casual atmosphere to wind down after the conference. The pool is located on the 2nd floor of the Kalia Tower at the Hilton Hawaiian Village.

Tuesday, 5 June **19:00-20:00**
MTT-17 Anniversary Reception **Hilton MPCC Coral 2**

Magnetic resonance imaging (MRI) is an important tool for medical diagnostics and other applications. It is also a major application of HF/VHF/UHF technology. To celebrate its tenth anniversary, Technical Committee MTT- 17 will present a talk on “Trends in Magnetic Resonance Imaging (MRI)” by J. Thomas Vaughn. Dr. Vaughn is a professor at the University of Minnesota and a recognized expert on the RF aspects of MRI. MTT members and guests are welcome.

Tuesday, 5 June **20:00-22:00**
Ham Radio Social **Hilton MPCC Coral 2**

All radio amateurs attending IMS 2007 are invited. Al Katz, W2UYH, will kick off the evening with a talk on earth-moon-earth communication, known as EME or moon bounce.

SOCIAL EVENTS (continued)

Wednesday, 6 June 18:00-20:00
Industry-Hosted Cocktail Reception Hilton MPCC Coral 3
Symposium exhibitors will host a cocktail reception. Complimentary beverage tickets will be included in the registration packages.

Wednesday, 6 June 19:30-22:00
MTT-S Awards Banquet Hilton MPCC Coral 4
The MTT-S Awards Banquet includes a fine dinner, awards presentation, and entertainment. Major society awards will be presented. Tickets can be purchased at the time of registration.

Thursday, 7 June 12:00-14:00
MTT-S Student Awards Luncheon HCC Ballroom C
All students are invited to attend the luncheon, which recognizes recipients of the IMS 2007 Student Paper Awards, MTT-S Graduate Fellowships, MTT-S Undergraduate Scholarships, and the Student High-Efficiency Power Amplifier Competition Prize.

Thursday, 7 June 17:30-21:00
IEEE MTT-S GOLD Reception and Luau Sheraton
Diamond Head Lawn
The IEEE MTT-S Graduates of the Last Decade (GOLD) Committee invites all GOLD members to a relaxing reception overlooking Waikiki Beach. Transportation will be provided from the Hawaii Convention Center to the Sheraton Waikiki. The reception will be followed by a luau located next door at the Royal Hawaiian Hotel. Tickets for the luau can be retrieved by GOLD members who complete a brief survey at either the IEEE MTT-S Membership-GOLD Booth or at the end of the IEEE MTT-S GOLD Committee sponsored Panel Session PTHA on "Career Development."

Saturday, 9 June 11:00-21:15
IMS 2007 Golf Tournament Ko Olina Golf Club
In the format of a four-man scramble, the tournament will take place at the Ko Olina Golf Club (www.koolinagolf.com), once recognized as one of Golf Digest's "Top 75 Resort Courses in the US." Individual and team prizes will be given after the tournament and attendees can choose to participate in a dinner after the awards are announced. Transportation departs Hilton Hawaiian Village and Sheraton at 11:00. Check-in at 12:00. Shotgun Tournament from 13:00-17:00. Register at www.mcahawaii.com/grps07/ims2007hi.

Hospitality, Guest Program, and Tours

Hospitality Suite

We offer two hospitality suites for the families of our technical attendees to relax and enjoy while experiencing everything that Hawaii has to offer. Both suites are open Sunday, 3 June through Friday, 8 June from 07:00 to 12:00 and offer a delicious breakfast and grab-and-go snacks, as well as assistance from our destination management company to aid you in booking tours. Both hotels offer exciting activities for your keiki (children). Please refer to the websites below for additional information and reservation procedures.

Hilton Hawaiian Village Hospitality Suite

Honolulu Suite (second floor of the Tapa Tower, overlooking the Tapa Tower Pool) Keiki program:

www.hiltonhawaiianvillage.com/activities/children-programs.asp

Sheraton Waikiki Hospitality Suite Niihau Suite

(second floor near the main elevators) Keiki program: www.sheraton-waikiki.com/act_keiki_aloha.htm

Guest badges are required for entry into both Hospitality Suites.

Guest Program and Tours

Aloha! We are pleased to provide all IMS and RFIC 2007 attendees and their guests with a wide variety of tours and other activities for your enjoyment during your stay in Hawaii.

We encourage participants to register before the conference via website (www.mcahawaii.com/grps07/ims2007hi), as we believe it is the most convenient option. MC&A may also be reached via email (ims2007hawaii@mcahawaii.com) or via fax at 1-808-589-5583. See www.ims2007.com for additional details.

Since Hawaii has so much more to see and do than what we have captured in the featured tours described here, additional tours and customized outer island vacation packages can also be arranged at the above website. The preconference registration deadline for all activities is 15.

Unless otherwise specified, prices include roundtrip transportation from the Hilton Hawaiian Village Tapa Tower bus depot and the Sheraton Waikiki bus depot.

One Day Maui Tour**Sunday, 3 June****05:00-20:00**

In Hawaii, they say “Maui No Ka Oi” – Maui is the best. Come and see why for yourself on an exhilarating motorcoach tour that takes you to some of the best sites on the island. From impressive natural wonders to sprawling, man-made, lavish resorts, the Valley Island of Maui has it all.

\$300.00 per adult, \$295.00 per child (2-11 years) includes: roundtrip transportation, roundtrip airfare (confirmed at time of reservations), admission to Haleakala National Park, state tax.

Kualoa Ranch**Monday, 4 June****07:10-14:00**

Experience the best land activities bundled into two exciting adventure packages. Located on Oahu’s northeastern shore, Kualoa Ranch rests at the base of two spectacular mountain ranges and has been the backdrop of such Hollywood blockbusters as Jurassic Park, Windtalkers, George of the Jungle, Tears of the Sun and the hit television series Lost. With the magnificent Koolau Mountains as your backdrop, it makes for the perfect setting for horseback tours, ATV tours, jungle expedition tours, a movie set tour and more!

\$94.00 per adult, \$59.00 per child (3-11 years) includes: roundtrip transportation, choice of up to 2 activities, and buffet lunch. Please see registration website for activities, age restrictions, and menu.

Arizona Memorial, USS Missouri, and City Tour**Monday, 4 June****06:30-15:30**

Celebrate the honor, valor and courage of the US Servicemen who served during World War II on this special Stars and Stripes tour. It’s a nostalgic journey to the two historic places that marked the beginning and end of the war for the United States – Pearl Harbor and the USS Missouri.

From Pearl Harbor, you’ll take a drive through metropolitan Honolulu and up to the Punchbowl Crater for a drive through the National Cemetery of the Pacific. After enjoying the serenity and spectacular view atop Punchbowl, you’ll wind through Downtown Honolulu for a cruise through its many highlights. \$55.00 per adult, \$35.75 per child (3-11 years) includes: roundtrip transportation, USS Missouri admission and guided tour, and state tax.

Hole in the Wall Lunch Tour**Tuesday, 5 June****09:45-14:00**

Featuring yummy food, fascinating history, and culinary decadence! Bring a big appetite for this tour! You'll taste, touch, and visit several different food gems and exotic ethnic restaurants that contribute to Honolulu's delicious melting pot. We asked Hawaii's best chefs what they like to eat on their day off, and here's what specialties they suggested you try: Hawaiian plate lunch, Chinese dumplings, local style grinds, pastry, Thai noodles, barbecued meat satay, Vietnamese summer rolls, bento boxes, Mediterranean, and Hawaii's mysterious crack seed. Your guide will answer all your food questions. You'll get valuable tips on how to make your Hawaii vacation more memorable. Prepare yourself for a fantastic day of eating behind-the-scenes in beautiful Honolulu! \$103.75 per adult/child includes: roundtrip transportation, lunch, state tax.

One Day Big Island/Volcano Tour**Tuesday, 5 June****06:00-20:00**

From raging volcanoes to serene snow-capped mountaintops, the Big Island of Hawaii is an island of extreme power and beauty. Come visit the legendary Volcanoes National Park to witness the workings of Madame Pele (Hawaiian goddess of fire). You'll trek through miles of recent lava flows at Kalapana and the mysterious Halemaumau Fire Pit.

A no-host lunch stop will be made at the Volcano House.

\$300.00 per adult, \$295.00 per child (2-11 years) includes: roundtrip transportation, roundtrip airfare (confirmed at the time of reservations), admission to Volcanoes National Park, state tax.

Shangri-La: The Honolulu Estate of Miss Doris Duke
Wednesday, 6 June**Trip # 1: 07:30-11:30 (Maximum 25 guests)****Trip # 2: 10:00-14:00 (Maximum 25 guests)****Trip # 3: 12:30-16:30 (Maximum 25 guests)**

Fiercely independent, rich beyond avarice, an international celebrity and socialite, activist and philanthropist, Miss Doris Duke, one of the wealthiest people in history was certainly a force to be reckoned with! Unbeknownst to the world, Miss Duke inconspicuously created a veritable palace of treasures on the southern shore of Oahu. Shangri-La, Miss Duke's Honolulu estate is now open to IEEE for a glimpse into the life of this extremely remarkable, private and fascinating individual.

\$65.50 per person includes: roundtrip transportation, admission to the Honolulu Academy of Arts, admission to Shangri-La, guided tour, driver/guide gratuity. Sorry, no children under 12 allowed.

Sea Life Park Luau
Wednesday, 6 June**18:00-21:00 (luau)****17:05-21:30 with optional bus pick-up**

Sea Life Park offers the island's most beautiful setting for a traditional Hawaiian Luau! Overlooking the ocean above Makapu'u Point, the Sea Life Park luau is held in an unparalleled location revealing breathtaking views of Rabbit Island, the historic lighthouse, and the cliffs adjacent to the park. Only at the Sea Life Park Luau can guests witness a spectacular night time dolphin show, enjoy delicious traditional Hawaiian food, and a sensational Polynesian Revue provided by the famed performers of Tihati . . . all of this in an easily accessible location. Luau price includes park admission, enabling guests to experience the daily shows, activities, and educational displays on the day of their luau or on another day within 30 days of the luau.

\$83.50 per adult, \$50.00 per child (4-12 years) includes: all-day admission to Sea Life Park, lei greeting, welcome drink, Polynesian Revue, luau buffet (see website for menu), state tax. Optional roundtrip transportation available for \$16.00 per person.

Grand Circle Island**Thursday, 7 June****08:15-17:30**

Get to know Hawaii from the inside out with an all-day tour that covers 120 miles of Oahu's best sightseeing spots. You'll circle the entire island, beginning with a tour of the stunning, world-famous Diamond Head Crater. For a close-up view of a seawater eruption, you'll visit Hawaii's own Old Faithful known as the "Blow Hole," where you'll witness oceanside water play at full force. Besides a stop at Sandy Beach — a favorite for body surfers, you'll venture to the most celebrated surfing zones in the world along the North Shore — Waimea Bay, Sunset Beach and the spectacular Banzai Pipeline. At Dole Plantation you will ride the pineapple express train and learn about the history of Hawaii's pineapple industry.

\$64.00 per adult, \$37.75 per child (4-11 years old) includes: roundtrip transportation, Pineapple Express train ride at Dole Plantation, choice of stroll through Plantation Gardens or Pineapple Garden Maze, state tax.

Tropical Ocean Fun Cruise**Thursday, 7 June****08:25-13:00**

Every day is summer in paradise! Take advantage of the beautiful Hawaiian sunshine and warm island waters aboard the Tropical Ocean Fun Cruise! You'll enjoy this longer cruise with more activities, including fishing, waterslide, giant water trampoline, kayaking, water toys and rafts, jumping plank, fish feeding and sun deck! Explore the Rainbow Reef with provided snorkel equipment, instruction and tours. And get your cameras ready for Green sea turtles, Spinner dolphins and flying fish too! After building up your appetite, eat your fill of a delicious BBQ lunch buffet freshly grilled on board by friendly Starlet crew and open soda bar!

\$76.50 per adult, \$50.00 per child (3-11 years old) includes: roundtrip transportation, BBQ buffet lunch (see website for menu), open soda bar, state and harbor tax.

Polynesian Cultural Center**Friday, 8 June****12:05-22:15**

Polynesia comes alive in a celebration of song, dance and culture at Hawaii's most popular attraction – Polynesian Cultural Center. Nestled along the island's scenic North Shore, this is one must-see event. Travel across the South Pacific in a day, as you take an escorted tour through seven authentic Polynesian island villages – Tahiti, Tonga, Fiji, Samoa, New Zealand, the Marquesas, and Old Hawaii. Meet real Pacific Islanders and see them demonstrate the arts and crafts of their native lands.

\$134.00 per adult, \$99.00 per child (3-11 years) includes: roundtrip transportation, admission, IMAX Theatre, evening show, luau dinner (see website for menu), and state tax. See website for upgrade package: \$134.00 per adult, \$99.00 per child (3-11 years).

Star Sunset Dinner Cruise**Friday, 8 June****16:30-20:00**

Embark across the waves on a romantic dinner cruise aboard the luxurious Star of Honolulu. Delight in your favorite tropical libation beneath a crimson washed sky as the Star takes you on an intimate journey along the quiet Waikiki coastline.

\$89.00 per adult, \$57.00 per child (3–11 years old) includes: roundtrip transportation, dinner (see website for menu), one drink, show, state and harbor tax.

RFIC Attendee Hotels

1. Ala Moana Hotel
2. Doubletree Alana Waikiki
3. Hawaii Prince Hotel
4. Hilton Hawaiian Village (Headquarters hotel)
5. Hyatt Regency Waikiki
6. Ohana Waikiki Malia
7. Ohana Waikiki West
8. Sheraton Princess Kaiulani
9. Sheraton Waikiki
10. Royal Hawaiian Hotel



IEEE

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Waxhaw, NC 28173

2007 RFIC Symposium

Honolulu, Hawaii
June 3-5, 2007



PROGRAM

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Information that will be helpful in completing this registration form can be found in this RFIC Program Book. Specific Items included are:

- IEEE and MTT-S Membership - p. 82
- Advance Registration Information - p. 83
- On-Site Registration Information - p. 85
- United States Visa Advisory - p. 87

Please Note: RFIC technical sessions are held on Monday and Tuesday. RFIC Registration includes continental breakfast, admission to RFIC Technical Sessions, RFIC Plenary and Reception (with spouse/guest), the IMS Plenary Session on Tuesday Mid-Morning, and the Industrial Exhibit on Tuesday-Thursday. RFIC Registration also includes RFIC Program/Abstract Book, Digest, and CD Rom.

Workshop and Short Courses are listed below:

	Session	Time	Title
Sunday, 3 June 2007	WSA	Full Day	Architectural Design and System Verification for Wireless SoC
	WSB	Full Day	Wireless Reconfigurable Terminals
	WSC	Afternoon	Optimum CMOS Integrated LNA Design Techniques for Handsets
	WSD	Full Day	Nanoscale RFIC Design Challenges and Foundry Solutions
	WSE	Full Day	System in Package Technologies for Cost, Size, and Performance
	WSF	Full Day	Advances in WiMAX RF Technology
	WSG	Full Day	Solid-State Power Invades the Tube Realm
	WSH	Morning	UWB Radio: From Building Blocks to SoC
	WSJ	Afternoon	Advances in Mixer Design for UWB Transceivers
	WSJ	Morning	RFID
	WSK	Afternoon	Emerging RFID and Wireless Sensors: Technologies and Applications
	WSL	Afternoon	SDR to Cognitive Radion
	WSM	Morning	24 GHz ISM-Band Communications
	WSN	Afternoon	Millimeter-wave/Quasi-millimeter-wave Highly-integrated Circuits
	WSO	Morning	Silicon CMOS PA from FR to mmWave
	WSP	Afternoon	Integrated Broadband Tuners for Satellite and Terrestrial Applications
	TSA	Full Day	RFIC Circuit & System Design Tutorial
TSB	Full Day	Analog and High-speed Circuit Design Solutions for Nano RF CMOS	
TSC	Full Day	Tutorial Workshop on RF and Microwave Filter Design	
TSD	Morning	SDR and Cognitive Radio – The Need for Reconfigurable RF Front-Ends	
Monday, 4 June 2007	WMA	Full Day	Advances in Active Device Characterization & Modeling for RF & Microwave
	WMB	Full Day	On-Chip/Off Chip DC, RF, and Microwave Measurement Modules
	WMC	Full Day	High-Speed Signal Integrity
	WMD	Full Day	Emerging Packaging Technology and Applications at Millimeter Wave Frequencies
	WME	Full Day	High-Q RF MEMS Turnable Filters
	WMF	Full Day	Theory and Design of Phase Locked Loops
	WMG	Full Day	Challenges of High Power Device Characterization and Modeling
	WMH	Full Day	High Power Issues of Microwave Filter Design and Realization
	WMI	Morning	Nonlinear Noise in Frequency Converting Systems
	WMJ	Afternoon	Will Wide Band-gap Power Transistors Render Silicon Power Transistors Obsolete?
	WMK	Morning	Ultrafast Analog-to-digital (A/D) Conversion Technique and its Applications
	TMA	Full Day	High-Frequency Characterization of Printed Circuit-Board Materials
	TMB	Full Day	Practical Analysis, Stabilization, and Exploitation of Nonlinear Dynamics
	TMC	Full Day	How to Do Business In Far East
TMD	Afternoon	Novel Materials for RF MEMS	
Friday, 4 June 2007	WFA	Full Day	Reconfigurable and Smart Antennas
	WFB	Full Day	Recent Advances in Electromagnetic Metamaterials
	WFC	Full Day	Low-cost, Integrated, Automotive and Industrial Radar Sensors
	WFD	Full Day	Advances in Imaging Radar Technology
	WFE	Full Day	Terahertz Device Characterization and Security Applications
	WFF	Morning	Wireless Local Positioning
	WFG	Afternoon	Wireless Power Transmission of Space Solar Power Generation
	WFH	Afternoon	Miniature, Electronically Tuned Filter Technology
	WFI	Morning	GaN Device and Circuit Reliability
	TFA	Morning	Microwave and Millimeter-wave Packaging and Manufacturing 202
TFB	Afternoon	Multi-Domain Physics Modeling of MEMS and NEMS	
TFC	Morning	Nanoelectronic Devices: RF Characterization, Modeling, and Applications	

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